Performance Analysis of PTP Components for IEC 61850 Process Bus Applications

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Abstract—New substation automation applications, such as sampled value process buses and synchrophasors, require sampling accuracy of 1 µs or better. The Precision Time Protocol (PTP), IEEE Std 1588, achieves this level of performance and integrates well into Ethernet based substation networks. This paper takes a systematic approach to the performance evaluation of commercially available PTP devices (grandmaster, slave, transparent and boundary clocks) from a variety of manufacturers. The “error budget” is set by the performance requirements of each application. The “expenditure” of this error budget by each component is valuable information for a system designer. The component information is used to design a synchronization system that meets the overall functional requirements. The quantitative performance data presented shows that this testing is effective and informative. Results from testing PTP performance in the presence of sampled value process bus traffic demonstrate the benefit of a “bottom up” component testing approach combined with “top down” system verification tests. A test method that uses a precision Ethernet capture card, rather than dedicated PTP test sets, to determine the Correction Field Error of transparent clocks is presented. This test is particularly relevant for highly loaded Ethernet networks with stringent timing requirements. The methods presented can be used for development purposes by manufacturers, or by system integrators for acceptance testing. A sampled value process bus was used as the test application for the systematic approach described in this paper. The test approach was applied, components were selected, and the system performance verified to meet the application’s requirements. Systematic testing, as presented in this paper, is applicable to a range of industries that use, rather than develop, PTP for time transfer.

Index Terms—Ethernet networks, IEC 61850, IEEE 1588, performance evaluation, power transmission, protective relaying, Precision Time Protocol, smart grids, time measurement

I. INTRODUCTION

Time synchronization has been used in substations for consistent event time-stamping for some time [1], [2]. This consistency is required when investigating power system incidents. More accurate time-stamping is now required for phasor monitoring and for digital process buses [3]. New time synchronization systems, such as the Precision Time Protocol (PTP) [4], are proposed as a means of achieving the high level of performance required by these new applications [5], [6]. PTP is a bidirectional networked time transfer protocol, and can be used with a variety of underlying network protocols.

The International Electrotechnical Commission (IEC) Smart Grid Vision and US National Institute of Standards and Technology (NIST) standardization “roadmaps” recommend the use of PTP for high accuracy time synchronization in substations and IEC 61850 for substation automation and protection [7], [8].

The IEC 61850 suite of substation automation standards provide an inter-operable communication model that meets existing needs, while supporting future developments as technology improves. IEC 61850 communication profiles are based, where possible, on existing international standards. IEC 61850-9-2 specifies the requirements for an inter-operable Sampled Value (SV) process bus.

This paper takes a systematic approach to determining whether PTP, when used with the recently published “power system profile” [9], is a robust means of synchronizing a SV process bus. The operating environment for substation automation is onerous, with any failure of the synchronizing system disabling SV based protection of high voltage transmission lines and transformers. SV merging units generate a large amount of data (5.5 Mb/s per merging unit, required for each three phase set of current transformers). The “error budget” is set by the performance requirements of the application. The “expenditure” of the error budget by each component is valuable information for a system designer. The component information is used to design a synchronization system that meets the overall functional requirements, which in this case is the synchronization of SV process bus sampling throughout a substation.

The methodology presented in this paper provides a series of tests that can be used by system designers to evaluate timing components. The quantitative performance data presented in Section IV demonstrates that such testing is effective and informative. A comprehensive test of each grandmaster with each slave clock identifies the relative merit of each device. Results from testing PTP performance in the presence of SV process bus traffic demonstrate the benefit of a “bottom up” component testing approach combined with “top down” system verification tests.

Power system applications for PTP have been presented in a number of papers [5], [10]. The commercial implementation of process bus substations using PTP to synchronize sampling [11] has made this use of PTP an area of interest [6], [12]. Synchrophasors enable wide area monitoring and control of power systems with the aim of preventing wide-spread outages, however stringent phase accuracy requirements demand accurate sampling. The use of PTP in this application has been
discussed by a number of researchers [13], [14].

Testing of PTP devices is not new, with transparent clock performance investigated by several groups [15]–[17]. Tests of the ability of transparent clocks to accurately measure the residence time of PTP messages have been described by Burch et al. [15] and Cosart [16], however these researchers used specialized PTP test equipment. The method presented in Section III uses a precision Ethernet capture card and a grandmaster clock, which is a more cost effective solution. The non-PTP traffic in a process bus is predominantly multicast, and this affects the queuing behavior of Ethernet switches, and therefore the results in this paper build upon the work of [16], [17].

Background information, including substation definitions and details of timing requirements, are presented in Section II. The experimental methods for assessing synchronizing performance and transparent clock operation are presented in Section III, and the corresponding results in Section IV. The impact of these results on PTP for process bus applications are discussed in Section V, with final conclusions presented in Section VI.

II. BACKGROUND

A. Substation Definitions

A “process bus” carries waveform measurements, digital status information, and transduced analog data from the high voltage equipment in a substation (for example bus bars, circuit breakers, isolators, earth switches, power transformers, current transformers and voltage transformers) to the substation automation system (SAS), and conveys commands from the SAS to high voltage equipment in the switchyard (e.g., circuit breakers, disconnectors and transformer tap changer controls), over a digital network. Merging units convert a signal proportional to the input signal (which may be analog or digital) into a standard data format for transmission over the process bus. The inputs to a merging unit may be conventional current and voltage transformers (in the case of a Stand Alone Merging Unit), or the output a non-conventional instrument transformers secondary converter.

Some protection schemes, in particular transformer protection, require inputs from multiple merging units or from process bus and conventional analog inputs. The current and voltage samples from different sources need to be synchronized by protection relays. Any synchronizing error, regardless of the method used, manifests as phase error, and this in turn results in “spill current” in differential protection schemes. This increases the chance of undesirable false tripping. Fig. 1 illustrates two examples of transformer protection where synchronization is required.

B. Synchronization Requirements

Process buses based on IEC 61850-9-2 must meet sampling accuracy requirements specified by IEC 61850-5 [18]. Table I lists the timing classes from edition 1 of this standard that are relevant to process bus networks, along with the proposed classes in the draft of edition 2. Protection class P2 is intended for transmission substation bays, and class P3 for transmission substation bays with high accuracy requirements. Class P1 is for distribution substations.

A widely adopted implementation of IEC 61850-9-2, termed “9-2 Light Edition” or “9-2LE”, specifies that sample synchronization use one pulse per second (1-PPS) signals, and that these have an accuracy that is better than 1 µs [19]. This, in combination with pulse propagation delays and sampling errors, ensures that overall sampling error is within the ±4 µs required by timing class T4/T5.

Phasor monitoring based on IEEE Std C37.118 requires that the total vector error (magnitude and phase) be less than 1% [20]. A synchronizing accuracy of 1 µs is proposed, as this allows for phase and magnitude errors in the source instrument transformers [2]. This aligns the synchronizing requirements of SV process buses and phasor monitoring, and sets the performance requirement that is used in this paper.

C. Performance Metrics

1-PPS synchronizing pulses are currently used to synchronize phasor monitoring units and merging units. The rapid update that such a signal provides makes jitter more significant than wander when looking at error. The direct comparison of 1-PPS outputs is a well established technique for evaluating the effectiveness of PTP for power system applications [6], [21]–[23]. Time errors are presented as time series, histograms, density functions, or a combination of these. This statistical analysis gives an understanding of the ongoing performance of the synchronizing system, and can identify operational aberrations. The errors may be between grandmaster and slave clocks, or between slave clocks synchronized to the same grandmaster. The use of PTP to synchronize a sampled value process bus is the focus of this paper, and therefore the “instantaneous” time error between the 1-PPS outputs of
grandmaster and slave clocks is the performance metric that will be used.

The “Correction Factor Error” (CFE) was defined by Burch et al. to be the difference between the actual residence time and the Correction field value [15]. A key observation was that a CFE that varies with latency indicates an error in the transparent clock’s estimate of the frame residence time. This metric is used in this paper to determine the performance of transparent clocks under a variety of network load conditions.

III. Method

The systematic approach to evaluating the performance of PTP devices uses a variety of tests. These tests can be applied to single devices, to the system as a whole, or a combination of the two. The tests described here are not exhaustive, and do relate to the application under investigation.

The test methods used to demonstrate the approach fall into two classes. The first class was assessment of 1-PPS synchronizing accuracy, and included grandmaster, slave, transparent and boundary clocks. These tests provided a methodology for system integrators to follow when evaluating products for substation clocks. The second class of tests examined the ability of transparent clocks to compensate for latency introduced by other network traffic on the shared process bus, in particular SV traffic in excess of 50 Mb/s.

The PTP parameters specified in Table 1 of the Power Profile [9] were used for these tests. The key parameters were 1 s update rates for Sync, Announce and PathDelay messages. Layer 2 multicast messages were used as the transport and the network speed was fixed at 100 Mb/s. The peer delay mechanism was used for path delay measurement.

Commercially available PTP devices were used in the development of these tests. The results in this paper provide a survey of performance, as well as demonstrating the application of the test methods. The grandmaster and slave clocks are represented by host names (PTP\text{x}), and the Ethernet switches are represented by a code letter (H, M, N and O). A total of three grandmasters, four slave clocks and four Ethernet switches (capable of transparent and boundary clock operation) were used in these tests.

A. Grandmaster and Slave Clock Sync Accuracy

The test method used to assess synchronizing performance is an established method, and uses the 1-PPS electrical outputs of the master and slave clocks. A digital oscilloscope (Tektronix DPO2014) sampling at 10^9 samples/s calculated the time difference (which is referred to as “delay” in these results) between the reference (grandmaster) and slave clock over a 30 minute period. A computer recorded each measurement (1800 in total for each test) for statistical analysis. Fig. 2 shows this arrangement. Various combinations of grandmaster and slave clocks were used to observe how the selection of clock device influences performance. A cross-over twisted pair Ethernet cable was used to connect the grandmaster and slave clock to eliminate the influence of other network traffic on synchronizing performance.

B. Effect of Transparent and Boundary Clocks

Peer-to-peer transparent clocks or boundary clocks that support the peer-delay mechanism are required to distribute PTP messages when the C37.238 power profile is used. Experiments were conducted that examined the effect these application specific Ethernet switches have on synchronizing performance.

The influence of each transparent clock and boundary clock was assessed by placing the Ethernet switch under test between the grandmaster and slave clocks, in place of the cross-over cable. No other network traffic was introduced to the switch, and switch management links were disconnected for the duration of each test. Each test ran for fifteen minutes, generating 900 1-PPS delay measurements. The grandmaster and slave clock used for these tests were the pair that had the best synchronizing performance when directly connected.

Ideally transparent clocks will estimate the path delays and frame residence times with minimal error. Errors in these estimates result in synchronizing error between grandmasters and slave clocks. Annex B of IEEE Std C37.238 specifies that the worst-case time error between the standard time source and a slave device be ±1 µs, with up to 16 network hops and 80% line-rate network traffic [9]. Grandmaster error is allocated ±0.2 µs and network error is the remaining ±0.8 µs. This limits each transparent clock to introducing no more than 50 ns of error in each of the 16 hops (15 identical transparent clocks, 1 grandmaster and 1 slave clock).

Fig. 3 shows the connections for the test with four transparent clocks. Two, three and four transparent clocks in series were each tested to determine the effect of cascaded switches, and to see if the standalone responses could be used to predict the behavior of cascaded switches. All Ethernet connections were fixed at 100 Mb/s, even though some switches supported 1 Gb/s. The four switches were also configured as boundary clocks, and tested using the same arrangements.
C. Estimation of Transparent Clock Residence Time

Rather than use a packet injection test set or specialized slave clock, the approach taken was to simultaneously capture the output of a conventional grandmaster using an in-line Ethernet tap (NetOptics 10/100/1000 Tap) and the output of the transparent clock under test with a precision Ethernet capture card (Endace DAG7.5G4), as shown in Fig. 4. The DAG card includes a precision time-stamping unit that was synchronized and synchronized (frequency locked) to the grandmaster’s 1-PPS output. This improves the DAG card’s time-stamping accuracy, and minimizes drift [24].

A third Ethernet port on the DAG card was used to inject multicast traffic into the transparent clock to simulate other network traffic. VLAN filtering was used to protect the grandmaster from the multicast traffic, and this is recommended practice with multiple multicast protocols in a process bus [25]. The multicast traffic was injected into the switches at 1000 Mb/s to simulate the simultaneous arrival of SV frames, thereby increasing latency, but the total load did not exceed 100 Mb/s. The exception to this was Switch M which only had Fast Ethernet ports, and therefore traffic injection was at 100 Mb/s.

The DAG card time-stamped the frames entering and leaving the transparent clock with a common clock, giving a measurement precision of 8 ns. The 1-PPS input to the DAG card is used for synchronization which improves the accuracy of the time-stamping clock. This could be supplied by a stable local 1-PPS source, such as a GPS receiver, enabling transparent clock performance to be measured in the field. This is a benefit of this method compared to those used in [15] and [16].

The DAG card combines frames captured from all ports into one “ERF” file. The PTP Correction field contents were extracted from PTP Sync and Follow-Up frames entering and leaving the transparent clock, and the change in the Correction field values calculated. This allowed for transparent clocks to be installed between the grandmaster and transparent clock under test, and for one or two step transparent clocks to be used. One step transparent clocks update the Sync message, while two step transparent clocks update the Follow-Up message.

Four different transparent clocks were tested, and five multicast network loads were applied to each transparent clock: no background traffic, six 9-2LE merging units, 21 9-2LE merging units, 25 Mb/s random length frames and 95 Mb/s random length frames. The length of the random frames was uniformly distributed between 64 and 1500 bytes. Eight PTP Sync messages were transmitted per second by the grandmaster and frames were captured for 10 minutes (approximately 4880 PTP Sync and Follow-Up messages). The sync rate was faster than that specified in C37.238, but enabled a greater sample size to be collected in a reasonable time.

D. PTP and Sampled Values

Results from testing the transparent clocks individually show that three of the four transparent clocks accurately estimated switch residence time. These three switches (H, M and N) were then connected in series and synthetic SV traffic was injected into the first transparent clock at 1 Gb/s to simulate the simultaneous arrival of frames from multiple merging units. Fig. 5 shows the arrangement of devices. 1-PPS delays between the grandmaster and slave clock were recorded for 15 minutes (900 samples for each test).

Prioritization and VLAN separation using IEEE Std 802.1Q tagging was used, with SV and PTP frames placed in separate VLANs. SV frames were assigned a priority of 4 for all tests. Two sets of experiments were conducted to determine the effect of load and priority on synchronizing performance:

1) The effect of SV traffic on PTP performance was assessed by injecting six levels of SV traffic into the test system: no traffic, 1 merging unit(MU), 3 MUs, 6 MUs, 12 MUs and 21 MUs. Previous testing has shown that 21 SV transmissions are the maximum that 100 Mb/s Ethernet can accommodate without dropping frames (for a 50 Hz power system). PTP frames had a fixed priority of 4 for the loading tests.

2) The effect of prioritization on PTP performance was examined by varying the 802.1Q priority of PTP frames while keeping the SV frame priority fixed at 4. Two levels of SV traffic were injected (12 MUs and 21 MUs) for each of the three PTP priorities: 2, 4 and 7.

IV. RESULTS

This section presents the results of the experiments described in Section III, and in the same order.

A. Effect of Clock Selection

The standard deviation and range of delays for each combination of grandmaster and slave clock are summarized in Table II. Time series plots for each grandmaster and slave clock combination are shown in Fig. 6, with a common y-axis.
range for all plots. The rows represent grandmaster clocks and the columns represent slave clocks in the table and the figure.

The results in Fig. 6 show that PTP devices intended for power system use are interoperable, as each grandmaster and slave clock combination successfully synchronized. The worst performing combination of grandmaster and slave clock, PTPD/PTPA, had jitter ten times worse than that of best performing combination, PTPC/PTPF. This shows that the clocks selected for a substation timing system influence its performance.

### TABLE II
SUMMARY OF JITTER IN GRANDMASTER/SLAVE CLOCK SYNCHRONIZING PERFORMANCE.

<table>
<thead>
<tr>
<th>Slave</th>
<th>PTPA</th>
<th>PTPB</th>
<th>PTPC</th>
<th>PTPF</th>
</tr>
</thead>
<tbody>
<tr>
<td>GM</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PTPA</td>
<td>81.2 ns</td>
<td>46.6 ns</td>
<td>69.4 ns</td>
<td></td>
</tr>
<tr>
<td>PTPC</td>
<td>77.9 ns</td>
<td>28.5 ns</td>
<td>—</td>
<td>6.58 ns</td>
</tr>
<tr>
<td>PTPD</td>
<td>101 ns</td>
<td>46.5 ns</td>
<td>41.7 ns</td>
<td>34.8 ns</td>
</tr>
</tbody>
</table>

(a) Standard deviation.

<table>
<thead>
<tr>
<th>Slave</th>
<th>PTPA</th>
<th>PTPB</th>
<th>PTPC</th>
<th>PTPF</th>
</tr>
</thead>
<tbody>
<tr>
<td>GM</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PTPA</td>
<td>705 ns</td>
<td>304 ns</td>
<td>798 ns</td>
<td></td>
</tr>
<tr>
<td>PTPC</td>
<td>715 ns</td>
<td>156 ns</td>
<td>—</td>
<td>42.5 ns</td>
</tr>
<tr>
<td>PTPD</td>
<td>670 ns</td>
<td>255 ns</td>
<td>232 ns</td>
<td>200 ns</td>
</tr>
</tbody>
</table>

(b) Range.

Fig. 7. Sample distributions showing the effect of transparent clocks on the best performing grandmaster/slave clock combination.

### B. Effect of Transparent Clocks

The majority of transparent clocks did not increase the jitter in the measured delay, but all transparent clocks other than switch M introduced an offset to the 1-PPS delay. Fig. 7 shows the distribution of 1-PPS delay for the four transparent clocks, with the direct-connect (cross-over cable) result included for comparison. Switch O introduced additional jitter to the distribution of delay, and the time series plot of the 1-PPS delay between grandmaster and slave clock in Fig. 8 shows a periodic disturbance. This cyclic pattern, present in a single transparent clock, suggests that there is a device specific issue and not a weakness in the standard. Selection of a grandmaster and slave clock that gave a 1-PPS delay that has low noise greatly assists the identification of perturbations introduced by transparent clocks, such as that identified in Fig. 8.
Fig. 8. Time series of 1-PPS delay with the best grandmaster/slave clock pairing, showing a periodic disturbance introduced by switch O.

C. Effect of Boundary Clocks

The transparent clock tests were repeated with the four switches in boundary clock mode, and the sample distributions of delay are shown in Fig. 9. The range of the x-axes in Fig. 7 and Fig. 9 are the same (215 ns) to aid comparison.

The jitter in the observed delay is similar to the directly connected case for each boundary clock. Switch O performs significantly better as a boundary clock, however the performance of switch M is degraded as a boundary clock.

D. Multiple Switches in Series

The four transparent clocks were connected in series, one by one, to assess the effect of multiple transparent clocks on synchronizing performance. Fig. 10 shows that one to three transparent clocks did not affect the offset significantly, but the fourth transparent clock did. It is significant that adding switch O to the chain increased the median delay by 434 ns, but when switch O was used by itself the median delay decreased by 114 ns. The offsets introduced by the transparent clocks do not appear to be additive, complicating system design. Performance testing of a PTP system should therefore be undertaken on the finished network, rather than combing the errors from the building blocks.

The four transparent clocks were reconfigured as boundary clocks to determine whether timing errors accumulated, resulting in degraded performance. The difference in performance between four transparent clocks and boundary clocks is significant, with the large offset present in the transparent clocks being eliminated. Switch O introduced significant jitter as a transparent clock, which is apparent in Fig. 7, but did not do so when operating as a boundary clock. The results shown in Fig. 11 suggest that switch O does not respond negatively to upstream clocks when in boundary clock mode. Further research is required to determine the optimum combination of transparent clocks and boundary clocks for the switches available in the process bus test bed.

E. Transparent Clock Correction Accuracy

The four network loads (six merging units, 21 merging units, 25 Mb/s random length frames and 95 Mb/s random length frames) increased the Sync message switch residence times. The no-load and 25 Mb/s random length frames cases have been selected to best demonstrate the effect of background traffic on latency and CFE. The other cases give similar results, with different ranges for latency. The random length frames represent TCP traffic on the process bus, which may be from a variety of sources. 25 Mb/s is equivalent to approximately six merging units.

Table III summarizes the results shown in Fig. 12. The mean and range of CFE did not vary when background traffic was added for switches H, M and N; however switch O’s CFE has increased range when the background traffic was applied. The CFE for switch O is dependent on latency, with the
negative slope apparent in Fig. 12 indicating the transparent clock is over-estimating the frame residence time (Correction exceeds the actual residence time). The slope of the point cloud is $-1.8 \times 10^{-5}$, suggesting the reference oscillator in this transparent clock is running fast by 18 parts per million. The $R^2$ (coefficient of determination) values in Table III confirm that switch O has some linear dependency between CFE and latency, and that switches M, M and N do not.

The residence time of Sync messages varies between the transparent clocks, and is listed in Table IV. This contrasts with latency observations of SV and GOOSE traffic (the traffic most likely to be on a process bus), where latency is similar between Ethernet switches. GOOSE messages vary in length, and generally carry binary and transduced analog information. Fig. 13 shows the latency distribution for 126 byte SV messages and 602 byte GOOSE messages.

Switch M is a one-step transparent clock, and was the one transparent clock that processed Sync messages as quickly as any other traffic of the same size (66 bytes). One-step operation requires special Ethernet hardware to manipulate the content of PTP frames as they are transmitted, and has not been widely adopted.

**F. Effect of Sample Value Traffic**

The transparent clocks that corrected estimated residence time were placed in series to represent a substation network topology, with bay level, voltage level, and core process bus switches.

Fig. 14 shows there is little variation in PTP performance as SV traffic levels increased from one to 21 merging units, and the observed differences are more likely to be natural variation in clock performance. It is significant that the “none” and “21 MU” sample distributions are the most similar, despite having the largest difference in SV traffic levels. Table V lists the total latency experienced by the PTP Sync message after passing through all three transparent clocks. Three outlier delays occurred, with all other latencies under 23 ms. The Correction field remained accurate, even at 657 ms, with a CFE of $-484$ ns.

Fig. 15 shows that at moderate load (12 MU, approximately 48 Mb/s) priority did not affect performance. However, at
TABLE V
LATENCY EXPERIENCED BY PTP SYNC FRAMES PASSING THROUGH THREE TRANSPARENT CLOCKS.

<table>
<thead>
<tr>
<th>SV Traffic</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>2.59 ms</td>
<td>16.1 ms</td>
</tr>
<tr>
<td>1 MU</td>
<td>2.59 ms</td>
<td>364 ms</td>
</tr>
<tr>
<td>3 MU</td>
<td>2.58 ms</td>
<td>187 ms</td>
</tr>
<tr>
<td>6 MU</td>
<td>2.57 ms</td>
<td>19.5 ms</td>
</tr>
<tr>
<td>12 MU</td>
<td>2.58 ms</td>
<td>15.3 ms</td>
</tr>
<tr>
<td>21 MU</td>
<td>2.59 ms</td>
<td>657 ms</td>
</tr>
</tbody>
</table>

high load (21 MU) higher priority PTP messages did yield slightly improved performance (an improvement of 5 ns over Priority 4), and the low priority case had marginally degraded performance (by approximately 18 ns). This result is contrary to established practice where PTP messages are thought to require high priority handling, however this does require the use of transparent or boundary clocks that support the peer-delay mechanism.

V. DISCUSSION
A. Effect of Clock Selection
The best performing grandmaster was PTPC, with the least jitter when used with any of the slave clocks. Similarly the best performing slave clock was PTPF regardless of the grandmaster used. These clocks had a range of local oscillator types, ranging in quality (from low to high) from a crystal oscillator (XO) in PTPA to an oven controlled crystal oscillator (OCXO) in PTPC. The slave-only clock PTPB had an XO and PTPF had a temperature compensated crystal oscillator (TCXO), and the difference in performance is apparent in Fig. 6.

The stability of an oscillator improves the phase noise, and higher Q improves performance (OCXOs have higher Q than TCXOs) [26]. PTP performance, as shown in Fig. 6, correlates with the expected phase noise performance of the local oscillator in each clock, based on the type of local oscillator.

B. Effect of Transparent and Boundary Clocks
Switches N and O performed better as boundary clocks, switch M performed better as a transparent clock and the performance of switch H was similar as a transparent or boundary clock. Switches that do not syntonize (frequency lock) their local oscillator with the grandmaster in transparent clock mode often do so in boundary clock mode, as their local oscillator becomes the reference for slave clocks and downstream boundary clocks.

The transparent clocks all supported boundary clock mode as an alternative to transparent clock mode. boundary clocks to some extent decouple slave clocks from the grandmaster, and can provide additional robustness in case of network outage if the boundary clock’s internal clock is sufficiently stable. transparent clock mode is the default for most switches, however the results presented in this paper show that boundary clock mode should be evaluated to ensure the best performance is obtained from the equipment in a PTP system. Designers need to be prepared to look at the boundary clock mode of operation when selecting products for a timing system.

Periodic perturbations in the synchronizing error between the grandmaster and slave clock with one transparent clock indicates that some implementations have issues. These perturbations are straightforward to observe when the synchronizing error is stable, but may be masked by a noisy grandmaster/slave clock combination. Therefore it is recommended that the most stable combination of grandmaster and slave clock is used for the assessment of transparent clock performance.

C. Transparent Clock Correction Accuracy
The mean CFE in Table III is not zero as the transparent clocks estimated the path delay with the peer to peer delay mechanism, and added this delay to the Correction field. The delay through the physical interface was as high as 300 ns for some PTP devices, giving peer-delays of 600 ns for short links. The latency measured by the DAG card through the Ethernet tap could not take into account delays leaving the grandmaster, and so the Correction field value was larger than the measured latency, resulting in the negative CFE values in Table III. Local oscillator frequency errors in transparent clocks have been shown to be the main source of error in
estimates of peer-to-peer path delay [27]. Synthesizing the local oscillators of transparent clocks to the grandmaster should improve the accuracy of residence time estimates, and this option is provided by some manufacturers.

The test methodology presented in this paper, using a standard grandmaster, an Ethernet tap and a precision Ethernet card, is a straightforward means of assessing the ability of a transparent clock to correctly measure the residence time of a PTP Sync message passing through the switch. This test could become part of a standard validation process for evaluating transparent clocks for substation timing, and can be applied throughout a substation.

D. Operation with Sampled Values

The results shown in Fig. 14 and Fig. 15 demonstrate that the PTP system performance meets the ±1 μs requirements of 9-2LE when a shared process bus network is used for SV and for time synchronization. Increased prioritization of PTP makes a slight improvement at high network loads, as the capability of transparent clocks to accurately estimate residence time compensates for queuing delays experienced by PTP frames. It has been suggested that PTP messages should be switched with high priority to ensure PTP accuracy [5], [17], but the results presented in this paper show that this is not necessary when peer-delay transparent clocks are used. PTP aware Ethernet switches operating as transparent clocks, with the exception of one, accurately measured the frame residence time of PTP Sync messages. This enabled PTP to provide acceptable synchronizing performance, with offsets less than 200 ns, in the presence of background traffic from 21 merging units. The one switch that had a latency dependent CFE introduced the most jitter when used in the timing network.

The switch residence time is not critical, provided the residence time is accurately reflected in the Correction field. The three large latencies of 187 ms, 364 ms and 657 ms show that accurate Correction values do compensate for large switch delays. Acceptable performance was obtained when all switches operated as a boundary clock. System integrators should consider this mode of operation when designing PTP timing systems for substations.

PTP and the power system profile meet the synchronizing requirements of SV process buses with a shared network, provided PTP-aware Ethernet switches are used.

VI. CONCLUSIONS

The methodology and results presented in this paper have demonstrated the benefits of a systematic approach to assessing the performance of a PTP based synchronizing system, with a particular focus on SV process buses in high voltage substations. Component testing, where each component is a commercially available PTP clock (grandmaster, slave, transparent or boundary clock), provides system designers with quantitative performance figures. The contribution of each device to the overall “error budget” can then inform product selection by customers, or product development by suppliers. “Top down” testing of the final application, such as SV process bus or synchrophasors, now becomes confirmation testing of acceptable performance, rather than a fault-finding process.

The results presented in this paper show that while all grandmaster and slave clocks tested were interoperable, a ten-fold difference in grandmaster-slave jitter existed between the best and worst performing combinations. Interoperability should not be underestimated as this is a significant concern when moving from established timing systems to new network based systems, such as PTP.

Gaining an understanding of how each component performs, along with overall performance, will provide decision makers the confidence to adopt this technology. Adoption of network based precision timing will reduce the cost of engineering and constructing substation automation systems, especially when the network extends to the high voltage switchyard.

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