DEVELOPMENT OF INNOVATIVE ROBUST STABILITY ENHANCEMENT ALGORITHMS FOR DISTRIBUTION SYSTEMS CONTAINING DISTRIBUTED GENERATORS

Hossein Sagha
B.Sc and M.Sc in Electrical Engineering

Submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

Electrical Engineering and Computer Science School
Science and Engineering Faculty
Queensland University of Technology
November, 2015
Keywords

Adaptive delay compensation, Clustering, Converter control algorithm, Distribution Static Synchronous Compensator (D-STATCOM), Dynamic Voltage Restorer (DVR), Feedforward, Frequency adaptive Phase-Locked Loop (PLL), Harmonic measurement, Internal Model Principle (IMP), Moving Average Filter (MAF), Online voltage regulation, Optimal DVR placement, PLL Modelling, Power quality improvement, Series voltage compensator, Synchronous Reference Frame (SRF), Voltage Source Converter (VSC)
Abstract

Low voltage (LV) residential grids were traditionally designed without consideration of renewable energy impacts. In other words, voltage drop was one of the main considerations in network planning with respect to the projected peak demand. For such design planning, the fixed tap at the secondary side of the distribution transformer is usually set between 1.02-1.05 pu in order to compensate high voltage drop during peak demand periods. However, as the network is growing and penetration of Distribution Generation (DG) units such as photovoltaics (PV) is increasing, the operation of networks is changing and voltage profiles in the network have been adversely affected. Voltage rise in high PV penetrated locations during midday and voltage drop during peak demand periods in the evening are becoming the main power quality issues for residential networks. As a current solution for overvoltage problem, if bus voltage of any PV inverter passes a pre-set limit, it will trip which causes loss of renewable energy. Additionally, non-linear loads inject harmonic currents into the grid leading to bus voltage quality degradation.

These problems are addressed in this research work. As a practical and economical solution, this thesis proposes voltage regulation and quality improvement algorithms for LV network operation. As part of these techniques, a Dynamic Voltage Restorer (DVR) as a series voltage compensator is designed and modelled for regulation and quality improvement in both high generation and high demand periods as well as for improvement of harmonic distortion in bus voltages. In the proposed method, a continuous and online control strategy adjusts the DVR output voltage to minimise bus voltage deviations in the entire network while reducing harmonic distortions. This maximises PV power injection by eliminating overvoltage trips and also provides voltage compensation for the peak demand voltage drop. In addition, it reduces the increased network demand caused by voltage rise at constant impedance loads which increases branch currents and consequently power losses.

One of the advantages of this method is that no communication link is required as the proposed algorithm uses the locally measured data of compensator in order to calculate a compensation voltage by using a provided equivalent line impedance (ELI) value for the downstream network of DVR. Avoiding communication links is
important as they are costly and prone to interruption, and introduce complexity into
the network. As the tap for LV distribution transformer is normally fixed, the
proposed algorithm can provide the same operation as On-Load Tap-Changer
(OLTC) for LV grids but with the benefit of continuous and online regulation as well
as harmonic distortion reduction. In order to achieve the best DVR performance, an
optimisation algorithm is also proposed using the hybrid of heuristic-based Particle
Swarm Optimisation (PSO) and Genetic Algorithm (GA). This algorithm uses
clustered load level of buses during a year to reduce the optimisation computations
for finding the best location and rating of DVR as well as the best tap setting for
distribution transformer to minimise the investment cost while maximising voltage
quality at all buses in the entire year. A sample LV network with PV generation is
selected in this thesis to study the effectiveness of the proposed approach.

Furthermore, converter control and synchronisation are critical for using the DVR in
the network, and therefore, proper algorithms for these issues are also proposed in
this thesis. In this respect, a control algorithm is designed for tracking of harmonic
voltage references with minimum error and high disturbance rejection using Internal
Model Principle (IMP) and feedforward. In addition, an algorithm is proposed to
preserve the stability and performance of the control system by compensating control
loop delay and adaptation of control parameters to plant parameter variations.
Furthermore, the synchronisation required by DVR controller is achieved by
developing algorithms based on the Synchronous Reference Frame Phase-Locked
Loop (SRF-PLL) and Frequency-Locked Loop (FLL). Some algorithms are proposed
for improvement of these methods for having better harmonic rejection and response
time. Furthermore, these methods are extended by proposed improved algorithms to
measure selective harmonic voltage angles and amplitudes, apart from those of
fundamental voltage. These measured values are used by the compensation and DVR
controller for the generation of compensating reference voltage for DVR.

The proposed algorithms in this thesis are simulated using PSCAD/EMTDC and
MATLAB platforms. Several simulation cases are considered, and the results are
presented to verify the effectiveness and performance of the proposed algorithms as
compared with the proposed methods in literature. For some of the proposed
algorithms, Hardware-in-the-Loop (HIL) tests have also been performed in order to
prove their feasibility.
# Table of Contents

Keywords .................................................................................................................................. i
Abstract .................................................................................................................................... ii
Table of Contents .................................................................................................................... iv
List of Figures ........................................................................................................................ vii
List of Tables .......................................................................................................................... xii
List of Abbreviations ............................................................................................................. xiii
Statement of Original Authorship .......................................................................................... xv
Acknowledgements ............................................................................................................... xvi

## Chapter 1: Introduction

1.1 Background and Motivation ........................................................................................... 1
1.2 Aims and Objectives ...................................................................................................... 4
1.3 Significance and Scope .................................................................................................. 5
1.4 Original Contributions ................................................................................................... 6
  1.4.1 Synchronisation Algorithm ............................................................................... 6
  1.4.2 Converter Control Algorithm ............................................................................ 6
  1.4.3 Voltage Quality Improvement Algorithm ............................................................ 7
1.5 Thesis Outline ................................................................................................................ 7

## Chapter 2: Preliminary Studies

2.1 Historical Background of Synchronisation Algorithms .................................................. 9
2.2 Historical Background of Converter Control and Adaptive Algorithms ....................... 12
2.3 Historical Background of Optimisation Techniques .................................................... 14
  2.3.1 PSO Variants ..................................................................................................... 18
2.4 Historical Background of Voltage Regulation and Quality Improvement Algorithm .... 22
  2.4.1 Generator Power Factor Control (PFC) .............................................................. 22
  2.4.2 Reactive Power Compensation ......................................................................... 23
  2.4.3 On-Load Tap-Changer (OLTC) ....................................................................... 23
  2.4.4 Generation Curtailment ..................................................................................... 24
  2.4.5 Energy Storage ................................................................................................. 24
  2.4.6 Harmonic Compensation .................................................................................. 24
  2.4.7 Proposed Method ............................................................................................... 25
2.5 Summary and Implications ............................................................................................. 25

## Chapter 3: Grid Synchronisation and Harmonic Measurement

3.1 Single-Phase SRF-PLL Structure ................................................................................ 27
3.2 Modelling of PLL ........................................................................................................ 30
  3.2.1 SRF Transformation Stage .............................................................................. 30
  3.2.2 Moving Average Filter (MAF) ........................................................................ 34
3.3 Design Of Controller .................................................................................................... 36
  3.3.1 Lead Compensator and Delay Compensation Predictor .................................. 36
  3.3.2 Feedforward Compensator ............................................................................. 37
4.8 Distributed Generators

4.2 Development of Innovative Robust Stability Enhancement Algorithms For Distribution Systems Containing Distributed Generators

3.3.3 Controller Tuning

3.4 Discretisation For Digital Realisation

3.5 Frequency Adaptive Moving Average Filter

3.6 SOGI-FLL With Harmonic Rejection

3.7 Phase Measurement for Selective Harmonics

3.8 Simulation Studies

3.9 Experimental Studies

3.10 Conclusions

Chapter 4: DVR Converter Design and Control

4.1 DVR Structure

4.2 DVR Protection

4.3 LC Filter Design

4.4 Modelling of The Converter

4.5 Modelling and Design of The Controller

4.6 Loop Delay Compensation

4.7 Adaptive Prediction Model

4.8 Simulation Studies

Development of Innovative Robust Stability Enhancement Algorithms For Distribution Systems Containing Distributed Generators
List of Figures

Figure 3.1 Block diagram of conventional single-phase SRF-PLL ..................................... 28
Figure 3.2 Block diagram of modified single-phase SRF-PLL ........................................... 30
Figure 3.3 Block diagram of SOGI-QSG ............................................................................ 32
Figure 3.4 Bode plot of SOGI, (a) $\alpha'$ component and (b) $\beta'$ component for different values of $k$ .................................................................................................................. 33
Figure 3.5 Bode plot of MAF (red) and the approximated transfer function (blue).......................... 35
Figure 3.6 Small-signal model of PLL ............................................................................. 36
Figure 3.7 (a) Open loop Bode plot and (b) step response of PLL to input phase change ...................................................................................................................... 41
Figure 3.8 Sampling pattern for digital realisation of PLL .................................................. 42
Figure 3.9 DF-II realisation of APF .................................................................................. 42
Figure 3.10 DF-II implementation of SOGI ...................................................................... 43
Figure 3.11 DF-I realisation of MAF ................................................................................. 45
Figure 3.12 Approximation for integration over a partial sample ........................................ 46
Figure 3.13 Illustration of the window resizing algorithm .................................................. 47
Figure 3.14 Block diagram of SOGI-FLL .......................................................................... 50
Figure 3.15 Bode diagrams of transfer functions of FLL input variables ......................... 50
Figure 3.16 Block diagram of integrated SOGI-FLL and SOGI-PLL for harmonic rejection ...................................................................................................................... 52
Figure 3.17 Block diagram of stacked PLL structure for selective harmonic measurement ....................................................................................................................... 53
Figure 3.18 Input signal and its fundamental harmonic ...................................................... 59
Figure 3.19 Response to a phase change at 300 ms followed by a frequency change at 400 ms, (a) measured phase, (b) frequency and (c) window length with PI-FF (blue) and PI-predictor (red)......................................................... 60
Figure 3.20 Response with uncompensated PI controller to a small phase change at 300 ms followed by a frequency change at 450 ms, (a) measured phase and (b) measured frequency .................................................. 61
Figure 3.21 Response to a frequency change without adaptive window resizing, (a) measured phase and (b) measured frequency with PI-FF (blue) and PI-predictor (red) ..................................................................................... 62
Figure 3.22 averaged and un-averaged $v_d$ and $v_q$ components with PI-FF controller ................................................................................................................................. 63
Figure 3.23 Response to a large phase change, (a) measured phase and (b) measured frequency ...................................................................................................................... 64
Figure 3.24 Response to a small delay at 300 ms followed by a 2 Hz frequency changes at 400 ms in the input signal, (a) measured phases and (b) measured amplitudes.......................................................................................... 65

Figure 3.25 Response to large delay at 300 ms in the input signal, (a) measured phases and (b) measured amplitudes............................................................................. 66

Figure 3.26 Responses to a voltage sag at 300 ms, (a) measured phases and (b) measured amplitudes.......................................................................................... 67

Figure 3.27 FLL response to a small phase change at 300 ms followed by a frequency change at 400 ms, (a) measured phase, (b) measured frequency and (c) window length ................................................................................................... 68

Figure 3.28 FLL measured phases in response to a short delay in the input signal at 300 ms followed by a 2 Hz frequency changes at 400 ms ............ 69

Figure 3.29 (a) measured phase and (b) measured frequency by the conventional FLL and with a fixed window length in response to a phase change followed by a frequency change ......................................................... 70

Figure 3.30 (a) HIL test configuration for PLL algorithm implementation, and (b) experimental setup ......................................................................................... 71

Figure 3.31 Ladder type DAC model in Typhoon HIL schematic editor with 4-channel selector ..................................................................................................................... 72

Figure 3.32 Realisation of circular array................................................................................................................................. 73

Figure 3.33 Realisation of compensated summation algorithm ................................................................................................................................. 73

Figure 3.34 Steady-state measured angles of harmonic voltages of the input signal in orange (0.5 V/div), (a) first and third harmonics and (b) fifth and seventh harmonics (60°/div) in blue and green, respectively............ 74

Figure 3.35 Response to a 10° step phase change, (a) measured phase (4°/div), and (b) measured frequency (0.5 Hz/div) ........................................................................................................................................................................ 75

Figure 3.36 Window length (2 samples/div) in response to a 10° step phase change ............................................................................................................................................................................ 76

Figure 3.37 Response to a 2 Hz step frequency change, (a) measured frequency (6.67 Hz/div) and (b) window length (3 samples/div) ................................................................................................................................. 77

Figure 3.38 Response to a 100° step phase change, (a) measured phase (40°/div), and (b) measured frequency (2 Hz/div) ........................................................................................................................................................................ 78

Figure 3.39 Window length (7 samples/div) in response to a 100° step phase change ............................................................................................................................................................................ 79

Figure 3.40 Response to a small delay in the input signal, first, third, fifth and seventh harmonic phases (35°/div) in blue, red, green and orange, respectively ............................................................................................................... 79

Figure 3.41 Response to a large delay, (a) first and third harmonic normalised amplitudes and (b) fifth and seventh harmonic normalised amplitudes (0.33 V/div), in blue and green, respectively ............................................................................................................... 80

Figure 4.1 Simplified schematic for grid connection loss ................................................................................................................................. 86

Figure 4.2 Diagram of DVR converter and feedback control ................................................................................................................................. 86
Figure 4.3 Envelope of the voltage and current ripples during half a mains cycle ................................................................. 89
Figure 4.4 Small-signal model of the converter ................................................................. 91
Figure 4.5 Sampling and PWM pattern during sampling intervals ............................... 95
Figure 4.6 Block diagram of the feedback control system ........................................ 95
Figure 4.7 Discrete-time block diagram of $R(z)$ .......................................................... 96
Figure 4.8 Transposed DF-II realisation of the resonant compensator ......................... 98
Figure 4.9 Implementation of stacked resonant compensators for harmonic tracking ................................................................. 99
Figure 4.10 Pole-zero map plots of resonant compensators for the closed loop (red) and the open loop (blue) transfer functions, and the arrows indicating the movement of poles ................................................................. 104
Figure 4.11 Pole-zero map plots for the open loop (blue), and the closed loop (red) transfer functions ................................................................. 107
Figure 4.12 open inner loop (blue), closed inner loop (red), and closed inner loop with delay (magenta) Bode plots ................................................................. 108
Figure 4.13 (a) Open loop Bode plot, and (b) closed loop bode plot ......................... 109
Figure 4.14 Output closed loop plot, and (b) closed loop (red) ........................................ 110
Figure 4.15 Sampling and prediction pattern ................................................................. 112
Figure 4.16 Block diagram of the control system with delay and predictor compensator ......................................................................................... 114
Figure 4.17 Output closed loop response to disturbance with (red) and without (blue) prediction of disturbance ................................................................. 116
Figure 4.18 Open loop Bode diagram without (magenta) and with (blue) parameters variations, and with adapted prediction model (red) ......................... 120
Figure 4.19 Open loop Bode diagram without (magenta) and with (blue) parameters variations, and with adapted prediction model and feedback coefficients (red) ................................................................. 123
Figure 4.20 Output closed loop response to disturbance without (magenta) and with (blue) parameter variations, and with adapted prediction model, feedback and feedforward coefficients (red) ......................... 123
Figure 4.21 (a) Transient response to the fundamental harmonic reference input, and (b) control effort ................................................................. 124
Figure 4.22 (a) Output and reference voltages, and (b) tracking error ......................... 126
Figure 4.23 Tracking error without the presence of disturbance current ......................... 126
Figure 4.24 (a) Output and reference voltages, and (b) tracking error without disturbance feedforward ................................................................. 127
Figure 4.25 (a) Output and reference voltages, and (b) tracking error without loop delay compensation ................................................................. 128
Figure 4.26 Tracking error with parameter variations, (a) without, and (b) with adaptation ................................................................. 129

Figure 4.27 Response with extreme parameter variations, (a) output voltage, and (b) tracking error ...................................................... 130

Figure 4.28 Response with adaptation to the extreme parameter variations, (a) output voltage, and (b) tracking error ................................ 131

Figure 4.29 Response to a load disconnection at 135 ms and reconnection at 160 ms ........................................................................... 131

Figure 4.30 DVR system emulation model in Typhoon HIL schematic editor .......................................................... 132

Figure 4.31 Steady-state response of output capacitor voltage (21.4 V/div) and transformer current (42.9 A/div) in orange and blue, respectively (2ms/div) ................................................................................. 133

Figure 4.32 Response in presence of extreme parameter variations ................................................................................ 134

Figure 4.33 Response in presence of extreme parameter variations and applied adaptive algorithm ......................................................... 134

Figure 5.1 Equivalent circuit of the traditional LV grid .......................................................... 138

Figure 5.2 Equivalent circuit of the LV grid with renewable energy units ... 138

Figure 5.3 Uniform single-line distribution network .......................................................... 140

Figure 5.4 Proposed structure for regulation of LV residential grid ........................................ 140

Figure 5.5 Sample non-uniform 6-bus network .................................................................. 141

Figure 5.6 Example of clustering applied to LDC for i-th bus ........................................... 141

Figure 5.7 Particle vector structure and included optimisation variables ........................................ 147

Figure 5.8 Optimisation flowchart .................................................................................. 151

Figure 5.9 Phasor diagram of the compensated network with DVR .................................. 154

Figure 5.10 Phasor diagram of the compensated network with DVR active power injection .................................................. 157

Figure 5.11 Open loop configuration for measurement of line current harmonics ................. 161

Figure 5.12 Block diagram of DVR reference voltage generation .................................. 162

Figure 5.13 Shunt voltage compensation using D-STATCOM ........................................ 163

Figure 5.14 Particle vector structure for D-STATCOM optimisation .................................. 163

Figure 5.15 Schematic of the network with DVR compensation ........................................... 164

Figure 5.16 Schematic of the network with D-STATCOM compensation .................................. 164

Figure 5.17 Bus voltage magnitudes in different load levels and with different tap settings, 0%, +2.5% and +5% ..................................... 168

Figure 5.18 Decision variables values as particle movement during the optimisation process .................................................. 170
Figure 5.19 Bus voltage magnitudes in different load levels without DVR (blue), and with optimised voltage and location of DVR for voltage deviation minimisation (red and green) ..................................................... 170

Figure 5.20 Decision variables values as particle movement during the optimisation process ................................................................................... 172

Figure 5.21 Bus voltage magnitudes in different load levels for DVR rating minimisation, without DVR (blue), and with optimised voltage and location for DVR (red and green) .............................................................. 172

Figure 5.22 Bus voltage magnitudes in different load levels with weighted optimisation, without DVR (blue), and with optimised voltage and location for DVR (red and green) .............................................................. 174

Figure 5.23 Bus voltage magnitudes in different load levels for deviation minimisation, without D-STATCOM (blue), and with optimised current and location for D-STATCOM (red and green) ....................... 175

Figure 5.24 Bus voltage magnitudes in different load levels for power rating minimisation with increased output current limit, without D-STATCOM (blue), and with optimised current and location for D-STATCOM (red and green) ....................................................................... 176

Figure 5.25 Open loop modelling of constant power injection ................................ 177

Figure 5.26 (a) bus voltage magnitudes and (b) deviation in load levels 2, 1, 3 and 4, respectively ..................................................................................... 178

Figure 5.27 (a) bus voltages, and (b) output power of PV inverter with overvoltage protection ............................................................................... 179

Figure 5.28 (a) Bus voltage magnitudes, and (b) PV inverter output power with active power curtailment ............................................................................ 181

Figure 5.29 (a) Bus voltage magnitudes, and (b) average bus voltage deviation with DVR in load levels 2, 1, 3 and 4, respectively ................................... 183

Figure 5.30 (a) DVR output reactive power, (b) DVR reference RMS voltage, and (c) DVR output voltage ........................................................................... 184

Figure 5.31 DVR output voltage and reference voltage ............................................. 185

Figure 5.32 (a) Voltage regulation with minimised DVR rating, and (b) average voltage deviation ........................................................................................ 186

Figure 5.33 DVR reference RMS voltage with minimised DVR rating ................. 186

Figure 5.34 DVR output reactive power with minimised DVR rating ..................... 187

Figure 5.35 (a) Bus voltage THDs and average THD with compensation using active power injection, (b) DVR compensating reference and output voltages, and (c) FFT of DVR output voltage ................................................. 188

Figure 5.36 (a) Uncompensated voltage, (b) compensated voltage, and (c) FFT for bus 5 voltage ........................................................................................................ 189

Figure 5.37 (a) Bus voltage THDs and average THD with compensation using only reactive power injection, and (b) FFT for bus voltage number 5 ...... 190
List of Tables

Table 3.1 Time response data for different SRF conversation stages .................. 34
Table 3.2 Control design results including time response and frequency
response data for different control structures ........................................ 40
Table 3.3 Time and frequency response data for different control structures for
harmonic stages .................................................................................... 57
Table 3.4 Amplitude and phase of the harmonic content of the input signal .... 59
Table 4.1 The parameter values for the designed plant .................................. 88
Table 4.2 Control design parameters .......................................................... 107
Table 4.3 Frequency response and transient step response performance .......... 111
Table 4.4 Control performance with plant parameter variations .................... 117
Table 5.1 Constraints of optimisation variables ........................................... 147
Table 5.2 Network parameters in different load levels ................................. 167
Table 5.3 Network branch parameters ......................................................... 167
Table 5.4 PSO-GA parameters .................................................................... 168
Table 5.5 Load flow analysis results for typical Network without DVR .......... 169
Table 5.6 Optimisation results for voltage deviation minimisation ................. 169
Table 5.7 Optimisation results for power loss minimisation ........................... 171
Table 5.8 Optimisation results for DVR rating minimisation .......................... 173
Table 5.9 Optimisation results for weighted objective function ....................... 173
Table 5.10 Optimisation results for different objective functions for D-
STATCOM ............................................................................................. 175
Table 5.11 Optimisation results for D-STATCOM rating minimisation .......... 176
Table 5.12 Nominal and curtailed active power generation at buses ............... 181
### List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analogue-to-Digital Conversion</td>
</tr>
<tr>
<td>AI</td>
<td>Analogue Input</td>
</tr>
<tr>
<td>AO</td>
<td>Analogue Output</td>
</tr>
<tr>
<td>APF</td>
<td>All Pass Filter</td>
</tr>
<tr>
<td>BCBV</td>
<td>Branch Current to Bus Voltage</td>
</tr>
<tr>
<td>BHCBHV</td>
<td>Branch Harmonic Current to Bus Harmonic Voltage</td>
</tr>
<tr>
<td>BIBC</td>
<td>Bus Injection to Branch Current</td>
</tr>
<tr>
<td>BIL</td>
<td>Basic Insulation Level</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>CV</td>
<td>Coefficient of Variation</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analogue Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DF-I</td>
<td>Direct Form I</td>
</tr>
<tr>
<td>DF-II</td>
<td>Direct Form II</td>
</tr>
<tr>
<td>DG</td>
<td>Distributed Generation</td>
</tr>
<tr>
<td>DI</td>
<td>Digital Input</td>
</tr>
<tr>
<td>DIMM</td>
<td>Dual in-line Memory Module</td>
</tr>
<tr>
<td>DLF</td>
<td>Distribution Load Flow</td>
</tr>
<tr>
<td>DO</td>
<td>Digital Output</td>
</tr>
<tr>
<td>DP</td>
<td>Dynamic Programming</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>D-STATCOM</td>
<td>Distribution Static Synchronous Compensator</td>
</tr>
<tr>
<td>DVR</td>
<td>Dynamic Voltage Restorer</td>
</tr>
<tr>
<td>ELI</td>
<td>Equivalent Line Impedance</td>
</tr>
<tr>
<td>EMTDC</td>
<td>Electromagnetic Transients including DC</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>FF</td>
<td>Feedforward</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
</tr>
<tr>
<td>FLL</td>
<td>Frequency-Locked Loop</td>
</tr>
<tr>
<td>FOH</td>
<td>First Order Hold</td>
</tr>
<tr>
<td>GA</td>
<td>Genetic Algorithm</td>
</tr>
<tr>
<td>GI</td>
<td>Generalised Integrator</td>
</tr>
<tr>
<td>HIL</td>
<td>Hardware in the Loop</td>
</tr>
<tr>
<td>HLF</td>
<td>Harmonic Load Flow</td>
</tr>
<tr>
<td>HV</td>
<td>High Voltage</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated-Gate Bipolar Transistor</td>
</tr>
<tr>
<td>IIR</td>
<td>Infinite Impulse Response</td>
</tr>
<tr>
<td>IMC</td>
<td>Internal Model Control</td>
</tr>
<tr>
<td>IMP</td>
<td>Internal Model Principle</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s Current Law</td>
</tr>
<tr>
<td>KVL</td>
<td>Kirchhoff’s Voltage Law</td>
</tr>
<tr>
<td>LDC</td>
<td>Load Duration Curve</td>
</tr>
</tbody>
</table>

Development of Innovative Robust Stability Enhancement Algorithms For Distribution Systems Containing Distributed Generators
Development of Innovative Robust Stability Enhancement Algorithms For Distribution Systems Containing Distributed Generators
Statement of Original Authorship

The work contained in this thesis has not been previously submitted to meet requirements for an award at this or any other higher education institution. To the best of my knowledge and belief, the thesis contains no material previously published or written by another person except where due reference is made.

QUT Verified Signature

Signature:

Date: 25/11/2015
Acknowledgements

First of all, I would like to express my earnest appreciation to my principal supervisor, Professor Arindam Ghosh for his support and guidance throughout my research studies. I also wish to extend my sincere appreciation and respect to my associate supervisors, Prof. Gerard Ledwich and Dr. Ghavameddin Noubakhsh, for their support, feedback and patience during this period. It has been a privilege for me to work under this supervisory team.

My appreciation also goes to Dr. Ali Arefi and Dr. Ghassem Mokhtari for their assistance and feedback. Furthermore, I wish to show my regards to ARC Australian Research Council (ARC) for their financial support during this PhD candidateship.

Last but not least, I express my gratefulness to my beloved wife, Maryam, from the deepest part of my heart. Without her pure love, absolute support and endless patience, I would not have been able to accomplish this research.
Chapter 1: Introduction

In this chapter, a brief introduction to the research problems is provided to indicate the motivations behind this research work. The defined aims and objectives for the research as well as significances and contributions of the research have also been stated. In the end, a brief outline of the thesis structure and research approach is provided.

1.1 BACKGROUND AND MOTIVATION

The utilisation of local renewable energy resources, such as photovoltaics (PV), as distributed generation (DG) units in low voltage (LV) grids around the world has had a dramatic increase. For example, in Germany, the nominal capacity of PV had increased to 34.8 GW at the end of August 2013 [1]. This high utilisation of PV in conventional LV grids brings new challenges to the network operators with bus voltage rise as the main issue due to the presence of line impedances throughout the network [2-4]. The study of UK distribution networks shows that overvoltage occurs between 25% to 30% PV penetration [5]. In order to deal with this issue, the current standards suggest that PVs need to be disconnected from the grid whenever the standard voltage limit is violated. Therefore, the loss of the renewable energy will be an inevitable result of voltage rise.

Additionally, due to demand growth in LV grids, the issue of voltage drop will be unavoidable in peak demand periods, where the voltage drop issue has unacceptable impacts on sensitive devices [3] and incurs reduced efficiency and stall of electric motors [6]. Additionally, constant power injection at buses increases branch currents and consequently power losses because of dropped voltage magnitude. The voltage drop issue can be dealt with by higher adjustment of distribution transformer tap setting which adversely adds to the voltage rise in the network and causes more loss of renewable energy. Therefore, by having a fixed tap setting both these problems cannot be resolved.

Traditionally, LV grids are designed to operate satisfactory during the peak load period. In other words, networks are planned such that all bus voltages fall within the permissible range, even during peak load periods. In this respect, the transformer tap
setting is normally set in the range of 1.02-1.05 pu. However, as PV penetration increases in the LV grids, their injection during high local generation periods usually causes a voltage rise. In such events, if bus voltage of any PV inverter passes a predetermined limit, it will trip. It is worth nothing that the tap of the LV distribution transformers is usually adjusted seasonally and is fixed during the operation. Therefore, ideally, with online voltage adjustment on the secondary side of the transformer, a great deal of voltage issues could be avoided. On-Load Tap-Changer (OLTC) is a solution but it incorporates limited discrete tap settings and cannot regulate bus voltages in a continuous manner in the distribution network. Reduction of harmonic voltages is not possible by this method as well. In addition, unlike voltage compensators, it can only adjust the voltage at the secondary side of the distribution transformer. All these issues prevent this method from having an optimum performance for minimising voltage deviations in the network.

As proposed in this thesis, a practical solution is utilising series voltage compensators in the network as Dynamic Voltage Restorer (DVR) which can be applied to traditional networks to overcome these issues. This compensator which is placed in series to the grid can push up or pull down bus voltage levels by injecting reactive and active power. Compensators can be distributed in the network in order to locally compensate bus voltages. However, it would be less costly and easier to manage, if one compensator with enough power rating was used to minimise bus voltage deviations. The compensator must be placed at an optimum location so that minimum required rating as well as minimum voltage deviations are achieved.

Moreover, nonlinear loads inject harmonic currents to the grid and introduce voltage distortions at buses. Elimination of these harmonics is possible by local harmonic compensation using series voltage compensators at buses [7]. However, by having a single compensator in the network, the harmonic distortion of bus voltages cannot be eliminated but can be reduced.

The compensation of fundamental voltage component and selective harmonic content must be performed online so that voltage quality improvement is always achieved during network operation for any demand and generation levels. This requires developing online and stable voltage regulation and quality improvement algorithms. Regulating bus voltages increases the efficiency of electrical networks and the renewable energy penetration. A reliable algorithm should not need any
communication links between buses and compensator because such links are vulnerable to interruptions and the reliability of compensation algorithm is endangered.

Furthermore, the compensator which is in fact a Voltage Source Converter (VSC) needs to be controlled to track a desired reference compensating voltage with minimum error and enough disturbance rejection. The control algorithm needs to be robust such that its performance and stability is preserved in different working conditions. Additionally, control of output for tracking selective harmonic reference voltages is an issue which can be dealt with by incorporating different control algorithms while all have their own benefits and drawbacks [8]. Control design based on Internal Model Principle (IMP) is a method for design of reference tracking algorithms in which stacked resonant compensators minimise the error in tracking a reference voltage containing harmonic references. This method theoretically has the benefit of eliminating the steady-state tracking error as well as full degree of freedom in placement of poles by adjusting the state feedback gains for tuning the control performance [9].

Additionally, issues of controllers including computation delay of digital controller and plant parameter variations, which adversely affect the control performance, need to be investigated and resolved. The solution for the former issue could be compensation of loop delay, using a model-based predictor which brings the problem of prediction model inaccuracy with presence of plant parameter variations. Therefore, by developing an adaptive algorithm, parameter variations can be considered, and their adverse effects are eliminated or reduced. The adaptive algorithm can be further extended to adapt the feedback and feedforward control coefficients to these parameter variations so that controller performance and stability are maintained.

DVR controller, however, needs to be synchronised with the grid voltage at its connection point and have information about the selective harmonic content of this voltage for the purpose of distortion compensation. This necessitates introducing stable and accurate algorithms for measurement of magnitude, angle and frequency of fundamental and harmonic components of a potentially highly distorted voltage. For this purpose, Phase-Locked Loop (SRF-PLL) and Frequency-Locked Loop
(SOGI-FLL) algorithms which are widely used for measurement of fundamental frequency content need to be improved and extended.

1.2 AIMS AND OBJECTIVES

The main objective of this thesis is to develop stability and quality enhancement algorithms for distribution networks which contain DG units. Investigating solutions for introduced adverse impacts of DGs and demand growth, including voltage regulation and quality problems, and utilising series compensators as a solution as well as considering practical aspects of using these devices, including synchronisation, converter control and stability, are the main focuses and aims of this thesis.

In order to achieve these objectives, different algorithms are developed and integrated throughout the thesis in order to deliver combined solutions for the above mentioned problems. Therefore, the following objectives are defined and addressed in this thesis.

- Development of synchronisation algorithm for measurement of disturbed grid voltage amplitude, angle and frequency for having a synchronised and stable operation of the voltage compensator.
- Extending the algorithm for selective harmonic measurement to be used for computations of selective harmonic compensation algorithm.
- Development of DVR converter control algorithm for tracking of a reference voltage including selective harmonic references with minimum error.
- Improving the control algorithm by compensating the control loop delay caused by computation delay and plant parameter variation effects on the control system.
- Development of an approach for fining an optimised location for DVR and an optimised configuration for distribution transformer in order to achieve the minimum voltage deviations in the network with minimum rating for DVR.
• Comparison of series compensation and shunt compensation using Distribution Static Synchronous Compensator (D-STATCOM) in order to justify the series compensation.

• Development of regulation and power quality algorithms for online compensation of network bus voltages and harmonic distortions while demand and generation levels at buses fluctuate.

• Comparison of the proposed algorithms with the existing proposed methods in literature.

1.3 SIGNIFICANCE AND SCOPE

The current solutions for the high voltage rise and drop problems caused by increased utilisation of renewable energy resources in LV grids introduce ineffective utilisation of renewable energy resources. These issues need to be considered, and an appropriate solution for both problems needs to be developed. This research work proposes the use of series voltage compensators in an optimum network configuration as a solution. Some other aspects of using these devices including synchronisation and control algorithms have also been investigated and designed in order to be integrated as a comprehensive solution for utilising these devices. In addition, the proposed approach in this thesis provides the following advantages:

• A single compensator with optimum rating and placement is considered for the voltage quality improvement of the whole network which reduces implementation, operation and electricity loss costs.

• Bus voltages are regulated online during network operation with variable demands and generations.

• PV units can inject their maximum available power with no voltage rise problem, and consequently, no loss of renewable energy is encountered.

• High bus voltage drops caused by demand growth in peak load periods are reduced, and their adverse effects on sensitive loads are eliminated.

• Harmonic distortion is also considered and a compensation algorithm is developed for reduction of harmonic distortion of bus voltages.

• Stable and proper operation of VSC is ensured by designing adaptive control and synchronisation algorithms.
1.4 ORIGINAL CONTRIBUTIONS

Based on the aims of the research, the contributions of the thesis for each part of the research are stated in the following.

1.4.1 Synchronisation Algorithm

- A synchronisation algorithm based on Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) is proposed and developed for measurement of angle and frequency of grid voltage in presence of harmonic distortion. The algorithm uses Moving Average Filter (MAF) for harmonic cancellation and is adaptive to frequency variations by a new method which is suitable for high sampling rates so that effective harmonic rejection is obtained in presence of grid voltage frequency variations.

- An improved model for the PLL structure is proposed which includes the response of system to frequency variations as well as phase variations.

- A feedforward method for improvement of large-signal operation of the algorithm is also proposed and designed.

- Algorithm is extended for selective harmonic amplitude and phase measurement with a new structure which needs limited number of harmonic stages by incorporating MAFs.

- Frequency-Locked Loop (FLL) structure is modified by using MAFs and integrated with PLL to form a new structure to be able to eliminate the error in frequency measurement caused by harmonic pollution and be able to measure the input signal angle as well.

1.4.2 Converter Control Algorithm

- An improved pole placement method for calculating state feedback coefficients is proposed for maximising the disturbance rejection while maintaining the desired stability margins.

- A model-based adaptive prediction method for the control loop delay compensation is proposed and designed. The compensation method can effectively compensate the computation delay of digital controller and
preserve the stability margins of the system in presence of plant parameter variations.

- An adaptive control system is proposed to maintain the stability and performance of control system in presence of plant parameter variations.

### 1.4.3 Voltage Quality Improvement Algorithm

- A new improved optimisation technique is proposed and developed in which practical objectives in the network, such as voltage deviation minimisation, can be achieved by finding optimum placement and sizing for DVR and D-STATCOM in the network as well as finding optimum tap setting for distribution transformer. The algorithm uses clustered bus load levels in order to reduce the optimisation computations.

- A new online regulation algorithm by incorporating DVR is proposed and designed in which only DVR locally measured data are required by the controller. Thus, in this method, no communication links between buses and DVR are needed for regulation of bus voltages while bus demands and generations are varying in the network.

### 1.5 THESIS OUTLINE

The remaining contents of this thesis are organised in five chapters. **Chapter 2** provides preliminary studies on synchronisation algorithms, converter control algorithms and voltage regulation and quality improvement algorithms in order to present the gaps and shortcomings in the previous related research. **Chapter 3** includes the design of synchronisation algorithms for grid-connected devices which are used for synchronisation of designed compensator to the grid voltage. Some different configurations for implementation of synchronisation algorithms are provided, and measurement of selective harmonic content is considered in the algorithms as well. Simulation and experimental results are also provided for verification of proposed algorithms. **Chapter 4** deals with design of the reference tracking control algorithm by which a desired reference voltage is tracked by converter output with minimum error. The design also includes the tracking of selective harmonic voltage references which is required for selective harmonic compensation. Provided simulation and experimental results verify the proposed algorithms. **Chapter 5** provides the optimisation approach in finding optimum rating
and placement of the voltage compensator in the network. Two type of compensators, shunt and series, are compared and the use of series compensator is justified. In addition, an online voltage quality improvement algorithm is provided in order to minimise network voltage deviations and be able to make the most of renewable generation and reduce electricity power losses. Effectiveness of proposed algorithms is verified by providing simulation results. **Chapter 6** is the final chapter which concludes the achievements of the research and provides some recommendations for future scope of the work.
Chapter 2: Preliminary Studies

This chapter includes the review of previous research studies relating to the scopes of this thesis. The aim of this chapter is to investigate and discuss research gaps and shortcomings with reference to research literatures to justify the motivations behind the research work conducted in this thesis. The research review investigates on synchronisation, control, optimisation and regulation areas which are provided in the following sections.

2.1 HISTORICAL BACKGROUND OF SYNCHRONISATION ALGORITHMS

Almost all grid-connected devices, such as battery or photovoltaic inverters as well as voltage compensators, require synchronisation with the fundamental frequency of the grid voltage which may be highly distorted by harmonics and have a limited variable frequency. Improving synchronisation speed and accuracy leads to enhanced accuracy and stability of device control algorithms. Many methods have been proposed in order to detect the frequency and phase of the grid voltage. Synchronous Reference Frame Phase-Locked Loop (SRF-PLL), which is a closed loop feedback control system, is widely used for this purpose because of its desirable performance, simple structure, and robustness in presence of signal distortions [10]. It can regulate the steady-state phase error to zero and is also able to measure the frequency of the input signal. In an SRF-PLL, the input signal is transformed to the synchronous reference frame in order to obtain the $dq$ components. However, these components for single-phase signals are obtained in the virtual synchronous reference frame by generating the orthogonal component of input signal. Various methods have been proposed for this purpose, including Second Order Generalised Integrator (SOGI), All Pass Filter (APF), transport delay, Hilbert transform, and inverse Park. All these methods have their own advantages and drawbacks [11-14]. SOGI has a limited bandwidth which reduces the harmonic content of the output while reducing the speed of conversion, but it is widely used and can be easily adapted to frequency variations [15-17]. Frequency response of APF has a flat unity gain, and therefore, harmonics are present at the output of the filter. Nonetheless, it has an easy implementation with a very low amount of computations. Transport
delay consumes some memory to store the previous samples of the input for the duration of a quarter of a period. Hilbert transform in not causal and it must be approximated by a causal finite impulse response (FIR) filter. Frequency response gain of this high-pass filter is strongly dependent on the filter order. In order to make the gain closer to unity, the order of filter must be increased [18]. This increases the conversion delay as well as the amount of required memory.

Besides, the generated $dq$ components are polluted with harmonic ripples. It is caused by DC and harmonic content of input signal and limited filtering capability of quadrature signal generator. A filtering method is required to attenuate or eliminate the harmonic ripples of the $dq$ components for which some modified versions of SRF-PLL have been reported. A low pass filter (LPF) as the loop filter can be effective in attenuating the harmonics, although it cannot eliminate them completely. Limiting the bandwidth of LPF reduces the amplitude of ripples while introducing more delay in the control loop. Therefore, notch filters (NF) have been suggested as an effective solution [19-21]. Moving Average Filter (MAF) which is a FIR notch filter is widely used because of its simple digital realisation and effectiveness in terms of the computational load [22, 23]. MAF filters out the periodic ripple content of $dq$ components, but it limits the loop bandwidth and reduces the response speed. Some methods like delay compensator [24, 25] and lead compensator [26] have been proposed for compensation of this delay. Another compensation method proposed in this thesis is using feedforward as an alternative method which can improve the performance in response to large phase variations. In [27-29] feedforward algorithms for other PLL structures are presented. However, in this thesis, feedforward is improved with respect to computational burden and is used to compensate the slow response of MAF.

MAF has also a frequency dependency problem, and for having an effective performance, its window length must be varied dependent upon the frequency of the input signal. Some adaptive methods based on variable window length and variable sampling rate have been proposed to deal with this problem [30-35]. In the variable length method, linear approximation of sample values is used when the window length is changed for the interval between two consecutive samples. This method is not accurate with low sampling rates and cannot be used with high sampling rates where window length must vary more than one sampling interval. On the other hand,
the variable sampling rate method has difficulty in digital implementation. Therefore, in this thesis, an improved and accurate frequency adaptive MAF is proposed which can be used with high sampling rates.

Furthermore, for proper PLL controller tuning, deriving a model of the PLL system is required. Small-signal modelling methods for SRF-PLL are presented in [21, 26, 30, 31]. However, they do not include the response to frequency variations which is a part of the frequency adaptive PLL. Additionally, the frequency response of single-phase virtual SRF transformation needs to be included in the model as well. Therefore, in this thesis, an improved modelling method for single-phase SRF-PLL is proposed which includes the response to both the phase and frequency variations of the input signal.

Apart from PLL, there is another structure called Second Order Generalised Integrator-Frequency Locked Loop (SOGI-FLL) which directly measures the signal frequency [15, 36]. This structure can also be extended with PLL to measure the phase as well. However, it will be shown in this thesis that harmonic pollution in input signal generates an error in the frequency measurement of FLL. Therefore, an improved structure is proposed which utilises MAF and PLL in FLL structure in order to eliminate the error caused by harmonics.

In addition to the fundamental component, harmonic measurement is essential for implementing selective harmonic compensation algorithms. In [21, 37-39] some harmonic measurement methods are provided which use stacked open loop stages for each selective harmonic frequency. These algorithms operate by eliminating the unwanted harmonic contents from input signal in each stage. However, since only limited selective harmonics are measured, all the harmonic content cannot be eliminated, and output ripples still exist in different stages. Therefore, for highly disturbed signals, numerous harmonic stages are required for effective elimination of harmonic content from input signal. In this thesis, an algorithm is proposed in which MAFs are used in closed loop selective harmonic stages to eliminate all the unwanted harmonic content so that effective elimination of harmonic ripples at output of stages is achieved.
2.2 HISTORICAL BACKGROUND OF CONVERTER CONTROL AND ADAPTIVE ALGORITHMS

The proper and stable control of compensator converters which inject reactive and active power to the grid is an important issue. The tracking error of fundamental and harmonic voltage references must be controlled to minimum, and the transient response must be fast enough for the application. All these criteria determine the accuracy requirements of the control algorithm, and they are summarised in [40] as: no phase and amplitude errors (ideal tracking) with high disturbance rejection, providing high dynamic response of the system, limited or constant switching frequency, low Total Harmonic Distortion (THD) and good DC-link voltage utilisation. Control algorithm must be able to satisfy all these issues as much as possible as well as being simple enough for realisation.

Many methods have been proposed for this purpose. Conventional PI controllers have fast dynamics, but they are able to eliminate the tracking error only in the synchronous reference frame ($dq$), and thus, harmonic tracking and rejection is limited.

Repetitive Controller (RC) and Proportional-Resonant (PR) controllers are developed based on the idea of Internal Model Principle (IMP) in which the compensator includes an internal model of the reference input in order to have zero steady-state error [41]. RC can eliminate the steady-state error in response to periodic references and disturbances. With this controller, high control loop gains at integral multiples of the fundamental frequency are achieved, and consequently, it can be used for harmonic reference tracking. RC controllers have slow dynamic response, but some variations of RC controller such as Proportional-RC and odd-harmonic repetitive controller have been proposed to improve the dynamic response [8]. PR controller is used when control variables are sinusoidal. It is defined directly in the stationary reference frame as,

$$G_{PR}(s) = K_p + K_r \frac{2\omega_c s}{s^2 + 2\omega_s s + \omega_0^2}, \quad (2.1)$$

where $\omega_0$ is the desired resonant frequency. $\omega_c$ is the introduced cut-off frequency for increasing damping factor to avoid problems in the discrete-time realisation related to pole placement at the border of the unit circle [42]. PR controller has a high gain
at around the resonant frequency, and thus, it can eliminate the steady-state tracking error effectively with good dynamics. Selective harmonic compensation with PR controller can be achieved by stacking several resonant controllers with specified resonant frequencies as,

\[ G_{pr}(s) = K_p + \sum_{h=1,3,5,...} K_{rh} \frac{2\omega_c s}{s^2 + 2\omega_c s + (h\omega_0)^2}, \]  

where \( h \) is the harmonic order. One advantage of this stacked configuration is that compensators do not affect the dynamics of each other because they only influence the frequency range in vicinity of their resonance frequencies [8]. Nonetheless, design of PR controller is difficult compared to PI controller because it is a multi-order compensator [43].

State feedback control is another approach in which state feedback gains are calculated based on the methods in multivariable control theory, such as pole placement or Linear Quadratic Regulator (LQR), to have sufficient damping [40, 41]. One of the benefits of this method is the full degree of freedom in placement of poles by adjusting the state feedback gains [42]. In this control method, the transient tracking errors are large, and there is a steady-state tracking error. Feedforward for both reference input and disturbance can be added to the system to reduce the transient and steady-state tracking error [44]. In addition, this method can be improved by considering the IMP. For the a sinusoidal reference input, a resonant compensator can eliminate the steady-state tracking error [45, 46]. Therefore, this improved structure has the benefits of both the resonant and state feedback controllers. Pole placement technique can be used for defining state feedback gains. As a proposed method for pole placement, [42, 47] suggest the placement of all poles on a circle with centre at the origin of the \( z \)-plane and with a radius close to unity. However, by using this method, achieving the maximum disturbance rejection, desired stability margins and desired transient performance simultaneously is hard, and therefore, in this thesis, an improved pole placement technique by modifying this method is proposed so that the desired performance is achieved.

Furthermore, an intrinsic problem of digital controllers is the time required for the control computations due to their limited working frequency. This computation delay, which is less than or equal to one sampling interval, reduces the phase margin
by introducing a phase lag to the control loop frequency response and may even cause instability. This delay can be included in the design of controller so that the bandwidth of system is reduced in order to compensate the phase lag at the unity gain frequency. This reduced bandwidth of control system is not desired and therefore, delay compensation methods based on linear extrapolation, phase lag compensation and model-based predictor have been proposed in [48-52]. The two former methods has the problem of added states to the system as well as the limited frequency range of compensation which makes them less efficient for design of high bandwidth controllers. There are also adaptive FIR filters implemented by Least Mean Square (LMS) algorithm as predictors [53, 54], but this method may have problem in convergence and stability of filter weights.

The model-based predictors such as Smith predictor [55] and Internal Model Control (IMC) [56] are two examples of model-based predictors which can be simply implemented. Ideally, by prediction of future values of plant currents and voltages for the duration of delay, the effect of delay is eliminated and the controller can be designed without considering the time delay. However, they rely on the model of the plant whose current and voltage values are predicted, and therefore, robustness of control may suffer from model uncertainties and parameter variations. Therefore, adaptation to plant parameter variations is necessary for maintaining performance and stability of system. Some adaptive methods have been proposed to deal with parameter variations for model-based prediction techniques [57]. Parameters of the plant, for instance the value of filter capacitor and inductor, can be estimated and updated dynamically by measuring the variation of current and voltages.

Therefore, in this thesis, a model-based prediction algorithm is used and an adaptive method is also proposed in which some correction terms are defined based on the estimated values of filter capacitor and inductor in order to modify the predictor model. An adaptive algorithm is also proposed to maintain the stability margins of the control system by modifying feedback and feedforward gains with correction terms defined based on the estimated plant parameter values.

2.3 HISTORICAL BACKGROUND OF OPTIMISATION TECHNIQUES

The electric power grid consists of synchronous generators, transformers, transmission lines, switches and relays, active and reactive compensators, controllers
and various constraints. Thus, it is a non-linear, non-stationary and uncertain system. In order to have various operation actions, design decisions and control objectives for the system, an optimisation problem needs to be defined and solved. Such a problem does not have a straightforward solution. In addition, first, the optimisation technique must be properly selected based on the nature of the problem. Secondly, all aspects of the problem must be considered. Thirdly, all the system constraints need to be included, and lastly, a comprehensive fitness or objective function which should not be too complicated must be defined [58]. In a simple form, the optimisation problem can be expressed as given in (2.3), where \( x \) and \( u \) are the decision variables, and the equality and inequality constraints are defined by \( g \) and \( h \) functions.

\[
\text{Objective Function } = \min \{ f (x, u) \},
\]
\[
\text{Subject to: } \begin{cases} 
g(x, u) = 0 \\
h(x, u) \leq 0 
\end{cases}
\quad (2.3)
\]

Various methods exist for solving the optimisation problems. The optimisation problems which are deterministic include some known parameters. Nevertheless, almost all the real world optimisation problems include some unknown parameters. Stochastic programming models are therefore required to include the probability distribution function of variables in the problem formulation. This technique is referred to as Dynamic Programming (DP) [58]. It is proven mathematically that DP can find an optimal solution for the problem and has been used for solving power system planning and operation optimisation problems [59-62]. However, this technique has some disadvantages. The DP algorithm cannot be solved in most of the optimisation problems. It also requires huge amount of computational effort which increases exponentially by the dimensions of the problem. These restrictions may result in a suboptimal solution [63].

Optimisation techniques which are based on computational intelligence, such as Genetic Algorithm (GA) and Particle Swarm Optimisation (PSO), can be used to overcome the issues of DP [58]. GA can find the approximate solutions to the optimisation problem as a search technique [64]. GA uses techniques inspired by evolutionary biology such as inheritance, recombination (or crossover), natural selection and mutation. It can find good solutions fast, in even complicated search hyperspaces. However, it has some disadvantages. GA tends to converge towards the
local optima, if the objective function is not defined properly. It also has difficulty in operating on dynamic data sets. In addition, other optimisation techniques may find better solutions in a specified computation time, for the same optimisation problem [58].

PSO is another evolutionary technique which was inspired by the social behaviour of swarm of insects. In PSO, a population of particles move through the problem hyperspace with velocities defined based on the exchanged information among the particles in order to find the optimal solution. Each particle is a candidate solution for the problem. The velocity of each particle, in each iteration step, is adjusted randomly according to the best position found so far by that particle and the best position among all the particles in the problem hyperspace. The ‘particle’s best’ and the ‘global best’ positions are defined by the evaluation of the objective function of the problem. Therefore, movements of particles evolve to an optimal or near-optimal solution [58].

PSO is not sensitive to the nonlinearity of the objective function or the number of decision variables and is able to converge to the optimal solution in many problems where analytical methods may fail to converge. In a power system, the optimisation problems are large-scale, mixed-integer and non-linear problems and exact mathematical methods can hardly be applied to solve them, and therefore, heuristic approaches, such as PSO, are widely used. Effectiveness of PSO in finding a solution to different optimisation problems in power systems has been shown [65-68]. Compared to other similar optimisation techniques, like GA, it has some advantages [58]. It is easier to implement and fewer parameters need to be adjusted. In addition, particles memorise their best value and the global best value which introduces a more effective memory capability. Furthermore, it is able to keep the diversity of the swarm. In GA, only good solutions are saved and the population is evolved around the group of best individuals. But in PSO, all the particles try to improve themselves by knowing the position of the best particle.

In PSO, a number of particles as $n$-dimensional vectors with random positions and velocities in the $n$-dimensional optimisation hyperspace are defined while each particle represents a candidate solution for the optimisation problem. The problem is finding a location for the voltage compensator with the minimum investment cost. The vector magnitudes in each dimension are decision variable values which include
location and voltage of the compensator. The problem is defined by a desired objective function as the minimum investment cost based on the decision variables. Particles estimate their fitness using this function, in each optimisation iteration step. Therefore, they have information about their own best fitness position found so far as well as other particles’ via exchange of information. Based on these data, they update their velocities and positions in the optimisation hyperspace such that finally they all converge to an optimum position. The vector magnitudes in each dimension in this position shape the optimisation solution.

The mathematical representation of the PSO approach is provided as follows. The position of the $i$-th particle in the $n$-dimensional real-valued problem space is defined by a vector as $\mathbf{x}_i \in \mathbb{R}^n$. The velocity of the particle is also a vector as $\mathbf{v}_i \in \mathbb{R}^n$ which defines the movement of particle in every dimension in each iteration step, $k$, as follows [69].

$$\mathbf{x}_i^k = \mathbf{x}_i^{k-1} + \mathbf{v}_i^k , \quad (2.4)$$

where,

$$\mathbf{x}_i^k = (x_{i1}^k, x_{i2}^k, \ldots, x_{in}^k) , \quad (2.5)$$

$$\mathbf{v}_i^k = (v_{i1}^k, v_{i2}^k, \ldots, v_{in}^k) . \quad (2.6)$$

Each particle has the knowledge of its best position found so far, $\mathbf{p}_i$, based on the evaluation of the objective function in the previous iterations as well as the information about the best position found so far by all the particles, $\mathbf{p}_g$. The relative importance of these two factors can be variable for different particles in different iterations. Therefore, a random weight is assigned to each part and the velocity is defined as,

$$\mathbf{v}_i^k = \mathbf{v}_i^{k-1} + \varphi_1 \mathbf{r}_{1i} \cdot (\mathbf{p}_i - \mathbf{x}_i^{k-1}) + \varphi_2 \mathbf{r}_{2i} \cdot (\mathbf{p}_g - \mathbf{x}_i^{k-1}) , \quad (2.7)$$

where $\varphi_1$ and $\varphi_2$ are acceleration constants and are two positive numbers. $\mathbf{r}_{1i}$ and $\mathbf{r}_{2i}$ are two $n$-dimensional vectors with random values uniformly distributed between 0 and 1. This equation has three components. The first one is the inertia component which models the tendency of particle to move in its previous direction. The second part is referred to as memory and defines the attraction of the particle towards its best position, $\mathbf{p}_i$, which has given the corresponding $p_{besti}$ value for the objective function.
The third one, which is referred to as cooperation, is the attraction of the particle towards the global best, \( p_g \), with corresponding fitness value of \( g_{\text{best}} \).

PSO is implemented iteratively by initialisation of a random distribution of a determined number of particles in the problem hyperspace at first. Then, in each iteration step, the fitness value for each particle is calculated and compared with the \( p_{\text{best}} \). If a better fitness is achieved, \( p_{\text{best}} \) is updated with this value and \( p_i \) is also updated with the current position of the particle. In addition, by finding the particle which gives the best fitness value, \( g_{\text{best}} \) is updated and \( p_g \) is located. Afterwards, the velocities and positions of all the particles are updated by using (2.4) and (2.7). This procedure continues until a stopping condition is met. The condition could be a maximum number of iterations, a sufficient fitness value or a maximum relative error for \( g_{\text{best}} \) or \( p_{\text{best}} \) of all particles in consecutive iterations. Some or all the above conditions can be checked simultaneously for the earliest one to be met.

The standard PSO has a tendency to become unstable and explode, if no limitation is put on the velocity of the particles [67] because of the stochastic characteristics of the velocity which creates an uncontrolled trajectory and makes the particles follow wider cycles in the problem hyperspace [70]. Therefore, in order to damp the oscillations, the velocities of particles in every dimension must be limited to \( \pm V_{\text{max } d} \), where index \( d \) denotes the \( d \)-th dimension.

### 2.3.1 PSO Variants

PSO can be improved by manipulating the acceleration constants or the inertia component of the velocity. In addition, PSO can be modified to be used for discrete-valued vector dimensions. Hybridisation of PSO with other evolutionary techniques has also been proven to be effective in improving the performance of PSO. All these modifications are described in this section.

**Inertia based Particle Swarm Optimisation**

In this method an inertia constant, \( w \), is multiplied by the inertia component of (2.7), as follows [71].

\[
\mathbf{v}_i^k = w \mathbf{v}_i^{k-1} + \phi_1 \mathbf{r}_{i1} \cdot (\mathbf{p}_i - \mathbf{x}_i^{k-1}) + \phi_2 \mathbf{r}_{i2} \cdot (\mathbf{p}_g - \mathbf{x}_i^{k-1})
\]  

(2.8)

The inertia constant can be a fixed term or can change dynamically. It can change the search behaviour of particles. A high value at the start of optimisation causes freer
movement of particles to find the global optimum region. After finding the region for the optimal solution, a low value for the parameter changes the search behaviour from explorative mode to exploitative mode in order to narrow the search region. However, the disadvantage of this method is that a decreased inertia weight holds the particles from searching the new regions [58].

**Constriction factor Particle Swarm Optimisation**

The update rule by this method is defined by (2.9) [72].

\[
 v_i^k = \chi \left[ v_i^{k-1} + \phi_1 r_{1i} \cdot (p_i - x_i^{k-1}) + \phi_2 r_{2i} \cdot (p_g - x_i^{k-1}) \right],
\]

where \( \chi \) is the constriction factor coefficient and is calculated as follows [72].

\[
\chi = \begin{cases} 
\frac{2\chi}{\phi_{\max} - 2 + \sqrt{\phi_{\max}^2 - 4\phi_{\max}}} & \phi > 4 \\
\sqrt{\chi} & \phi \leq 4
\end{cases}
\]

(2.10)

\( \chi \) is a constant between 0 and 1. Typically, \( \phi_{\max} \) is set to 4.1 to have a stable optimisation process [58, 72], and the acceleration coefficients which must meet (2.11) are typically chosen to be equal numbers as 2.05.

\[
\phi_1 + \phi_2 = \phi_{\max}
\]

(2.11)

Convergence of particles is improved over time by using this method. Because it damps the oscillations once the particle moves towards the optimal point in an optimal region. Moreover, this method has better performance compared to the inertia weight approach [73] and does not require velocity limiting for convergence [72].

**Discrete PSO**

The concept of optimisation can be extended to discrete-valued search spaces as well as the real-valued ones where particle vectors include discrete values in some dimensions. When the discrete values are integer, this is possible by rounding off the real values to the nearest integer in each iteration [74]. Therefore, first, by using Equations (2.7) and (2.4), the new real-valued position for the particles are calculated as \( x_i^k \in \mathbb{R}^n \). Then, the values of integer dimensions are rounded by using (2.12).
where \( d \) is the dimension of an integer-valued variable.

**Hybrid PSO**

In some cases, premature convergence and poor fine-tuning of the final solution, because of local optima, can occur in PSO. Therefore, PSO can be evolved by combining the strengths of PSO and other evolutionary techniques. One of the most common hybridisation methods is the use of GA in PSO. Selection, crossover, and mutation have been used in the PSO algorithm in order to improve the diversity of the population during optimisation and by means of that, escape from local optima [58, 66, 75].

Crossover which involves the reproduction and recombination of genes and is also referred to as breeding is a powerful aspect of the GA. In order to implement the crossover, a set of parent particles are selected for crossover after the location of particles are updated in the iteration step. The set is randomly chosen with a defined probability of selection which is referred to as crossover probability. Then, two random particles are selected from the parent population for crossover, \( \text{parent}_1 \) and \( \text{parent}_2 \). This is repeated until all the parents in the population are chosen. The parents are then replaced by their children, \( \text{child}_1 \) and \( \text{child}_2 \), and thus, the population size remains constant. The children’s positions are calculated by using arithmetic crossover for the parents’ positions, as follows [76, 77].

\[
\begin{align*}
\text{x}_{\text{child}_{1}}^{k} &= r_{x}^{k} \cdot \text{x}_{\text{parent}_{1}}^{k} + (1 - r_{x}^{k}) \cdot \text{x}_{\text{parent}_{2}}^{k}, \\
\text{x}_{\text{child}_{2}}^{k} &= (1 - r_{x}^{k}) \cdot \text{x}_{\text{parent}_{1}}^{k} + r_{x}^{k} \cdot \text{x}_{\text{parent}_{2}}^{k},
\end{align*}
\tag{2.13}
\]

where \( r_{x} \) is a vector of random values uniformly distributed between 0 and 1. The crossover of parent’s velocity vectors, as suggested in [76], can be performed by calculating the sum of parents’ velocity vectors and normalising the result to the original length of each parent’s velocity vector. Thus, each parent affects the direction of each child’s velocity vector equally, and by normalisation, the velocities of children are avoided from becoming too fast or too slow. However, a crossover approach similar to the one used for the positions is proposed for use in this thesis and applied to the velocity vectors, as follows.
\[
\begin{align*}
\mathbf{v}_{child_1}^k &= r_v^k \cdot \mathbf{v}_{parent_1}^k + (1 - r_v^k) \cdot \mathbf{v}_{parent_2}^k, \\
\mathbf{v}_{child_2}^k &= (1 - r_v^k) \cdot \mathbf{v}_{parent_1}^k + r_v^k \cdot \mathbf{v}_{parent_2}^k,
\end{align*}
\]  

(2.13)

where \( r_v \) is a vector of random values. By using crossover, the offspring particles have the partial properties of the parents and benefit from both of them. The arithmetic crossover of positions in the search hyperspace distributes the children in the space extended across the parents’ positions. This lets the particles to examine the search space between particles. For instance, if two parents are located at two different local optima, a crossover could lead to a escape from the traps and potentially find a better optimum position. In addition, the method used for velocity crossover benefits from partial selection of parents’ velocity properties in a random manner. This improves the diversity of velocities during optimisation which may lead the particles to a better optimum position. Nonetheless, even if optimisation escapes from local optima, in different optimisation executions it may find more solutions to the problem. These suboptimal solutions may be close to the optimal one in the objective function value, and the difference can be overlooked. Therefore, any of the solutions can be selected as the desired solution based on other criteria which have not been considered in the objective function.

Use of different optimisation techniques in finding the minimum investment cost by optimum placement and sizing of series and shunt compensators have been reported in [78-82]. However, they do not consider different loading conditions in the network. In this thesis, in order to consider the different loading conditions in a computationally efficient form, an optimisation approach is proposed in which clustered load levels of buses in a year are considered. The utilisation rates of clustered load levels are used to weight the objective function so that their influence on the optimisation is proportional to their duration. This results in a more optimum sizing, and therefore, reduced investment cost for the compensator. In addition, in this thesis, the effect of distribution transformer tap setting on optimisation is also considered. This parameter can also be defined as a decision variable, because depending on the clustered load levels of the buses and their durations, a more optimum solution could be achieved with a fixed tap setting of higher or lower than 1 pu.
2.4 HISTORICAL BACKGROUND OF VOLTAGE REGULATION AND QUALITY IMPROVEMENT ALGORITHM

The issue of voltage level fluctuations in distribution networks has become important with increasing number of DG penetration. The increasing generation level results in voltage rise above the permissible level [83]. IEEE standard for grid-connected PVs suggests that PV inverter should be disconnected in maximum time of 120 cycles, if its bus voltage passes the upper limit [84]. Therefore, the amount of renewable energy generation is limited by voltage rise. This necessitates developing algorithms for active management of distribution network. Current active network management plans can be categorised as centralised (or coordinated) control, semi-coordinated and decentralised (or distributed) control strategies [85].

Centralised control strategy uses a wide range of communication links from the substation to the rest of the network in order to coordinate different devices in the network, such as On-Load Tap-Changer (OLTC), static VAR compensator (SVC) and voltage regulator, to provide voltage regulation. Therefore, they provide wide coordination but require high implementation cost and extensive control [85]. The simplest algorithm based on this approach is coordinated voltage level management to adjust the substation voltage by changing the set point of the automatic voltage regulator relay based on the maximum and minimum voltages in the distribution network [85].

On the other hand, the two other types of strategies, semi-coordinated and distributed control, control DG unit locally while coordinating the unit with a limited number of network devices [85]. These strategies can improve the overall network regulation with reduced cost for communication links as well as fast response to rapid local voltage variations [86]. Additionally, local control avoids the need for design of an extensive control. The proposed methods for these strategies include power factor voltage control method, reactive power compensation method, OLTC, generation curtailment and storage [87] which are reviewed as follows.

2.4.1 Generator Power Factor Control (PFC)

If the amount of injected or absorbed reactive power by DG is controlled to compensate voltage variations caused by active power injection, voltage fluctuations can be maintained within the standard limits [88, 89]. For this purpose, three modes of operation on a rule based algorithm, including unitary, inductor and capacitive
power factors, are considered in [90]. However, IEEE standard for grid-connected PV recommends a power factor close to unity and does not let the utilisation of local reactive power control for voltage support in low voltage (LV) distribution networks [84]. Another drawback is that inverters must have larger VA capacity so that they can provide the required amount of reactive power.

2.4.2 Reactive Power Compensation

In this method, reactive power compensators are used to inject or absorb reactive power to the network for voltage compensation. The examples of these devices are SVC, Distribution Static Synchronous Compensator (D-STATCOM) and Dynamic Voltage Restorer (DVR). SVC is able to provide voltage regulation for a wide range of demands and DGs. The two latter ones have the advantage of fast response time and thus providing dynamic voltage control in the network [85]. However, for more effective reactive compensation during all possible system conditions compensators need to be coordinated [91, 92].

The operation is similar to PFC, but compensators provide independency from DG units, and a single compensator can be utilised for compensation of voltage rise caused by multiple DG units. DVR is a series compensator and is able to tightly regulate the voltage at the load side and compensate voltage sags and swells at the load [93]. It can also be used to inject harmonic voltages to cancel out harmonics at the load. DVR has good bandwidth and attenuation properties compared to D-STATCOM [94].

2.4.3 On-Load Tap-Changer (OLTC)

Fixed tap setting for distribution transformer can compensate either the voltage drop caused by high demands with a high tap setting or the voltage rise caused by high generations with a low tap setting. Seasonal tap adjustment may improve network voltage deviations to some extent but it cannot cover both these conditions which may happen hourly. Therefore, a common method for voltage control is to maintain an appropriate secondary voltage level by altering between multiple tap settings automatically with a voltage controller relay. Tap change occurs when the voltage crosses a pre-set limit. It also compensates the additional voltage deviation between the transformer and load location at the far end of the feeder [87]. A main disadvantage of this method is the limited tap settings. In addition, an intentional
time delay of 30 to 60 seconds is implemented in OLTC in order to prevent unnecessary tap changes during transient voltage fluctuations. It also takes a long time to move from one setting to another and also between frequent operations [87]. In addition, for high DG penetration, coordination between DG outputs and OLTC tap control is required [95, 96].

2.4.4 Generation Curtailment

Due to lack of flexibility in voltage control algorithms, trip of PV inverter is a solution in case of overvoltage. This wastes the potential renewable energy and reduces the efficiency of PV investment [97]. Local active power curtailment by reducing the amount of active power injection reduces the voltage rise. In [4, 98] droop based curtailment methods are proposed in which the generated active power is adjusted according to the local bus voltage to limit the voltage rise and prevent the overvoltage. Droop control technique results in sharing of power injection reduction among all the inverters in the network [85]. The drawback of this strategy is the loss of renewable energy generation which is not desirable for future grid.

2.4.5 Energy Storage

Energy storage technologies such as lead acid batteries and Pumped hydro are technically and commercially mature and are used widely is power systems [87]. Such devices provide a reserve for excessive renewable energy. Therefore, both active and reactive power can be sourced from or sunk to these devices for short or medium term compensation of voltage variations. Reference [1] proposes a local control for PV-storage system to avoid the voltage rise in the network. However, current high investment cost for energy storage systems makes it uneconomical for the present state of distribution networks.

2.4.6 Harmonic Compensation

In addition to voltage regulation, harmonic compensation using DVR has reported in [7, 99, 100] where the compensator is placed locally at the load bus to improve the Total Harmonic Distortion (THD) of bus voltage. Local D-STATCOM placement at non-linear loads has also been reported for absorption of harmonic current injection of the load to the network [101]. DG inverters are also used for this purpose by absorbing and circulating the harmonic current injection at DG bus [102, 103].
However, available DG rating can limit the harmonic compensation, and distributed compensation by D-STATCOM is not cost and maintenance effective.

2.4.7 Proposed Method

The proposed approach in this thesis is a decentralised control method in which no coordination and communication links are required. Additionally, this approach can provide optimised and online voltage regulation for a network by a single compensator. Reactive power compensation is achieved by series voltage regulation using DVR, which is more effective than shunt regulation using D-STATCOM. Online voltage regulation by estimating the average bus voltage deviation in the network has not been reported in the literature. It can minimise the average voltage deviation in the network with a single compensator as a cost and maintenance effective solution. Additionally, using the already inserted DVR in the network, THD reduction of downstream bus voltages can also be achieved.

2.5 SUMMARY AND IMPLICATIONS

It is implied from the literature that it is necessary to enhance voltage quality improvement algorithms because of the disadvantages of the already proposed algorithms. They may be not cost effective, may need coordination, cannot minimise the voltage deviations in the network and may not be allowed by standards. On the other hand, power quality enhancement by DVR has some advantages which make it a promising solution for future networks, at least as an intermediate step for a long haul. It is more effective than shunt compensation and can be inserted in an optimum location in the network for minimum investment cost. In addition, by devising a power quality improvement algorithm which does not need coordination between the compensator and the network buses and is able to minimise voltage deviations, a cost effective and reliable solution can be obtained.

In addition, the application of DVR in the network needs an improved design for the converter control and synchronisation algorithms as already stated in this chapter. Some of the required improvements include an improved algorithm for stable control of DVR converter in the grid in the presence of grid current disturbances as well as an improved algorithm for synchronisation of DVR converter in presence of voltage harmonics and frequency variations in the network.
In this chapter, a Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) is designed. An improved modelling compared to previous studies is provided for the structure so that the effect of frequency variations as well as phase variations is considered in the model. The proposed PLL structure is able to reject the harmonic content of the input signal by using Moving Average Filter (MAF), and extract the angle and the frequency of the fundamental component. In addition, the frequency dependency of MAF is resolved by a proposed algorithm in order to adapt it to input signal frequency variations so that it can effectively reject the harmonics in presence of input signal frequency variations. Compared to previous studies, it is adaptive to a wider range of frequencies even with a high sampling rate.

In addition, the effectiveness of feedforward in compensation of the slow response of MAF is also illustrated and compared to existing methods. Moreover, the design is extended to measure the voltage angle and amplitude of harmonic contents of the signal. The data will be used in converter control algorithm to synchronise the converter with the grid voltage and its harmonic content. The information is also required by the voltage quality improvement algorithm for proper compensation. Unlike the previous studies, the harmonic measurement algorithm by MAF is able to provide ripple free outputs with limited number of harmonic stages.

Moreover, the problem of Frequency-Locked Loop (FLL) structure in harmonic rejection is explained and an algorithm is provided without the need for harmonic measurement and cancellation in order to reject the harmonics. The simulation and experiential results are provided to illustrate the effectiveness and the performance of the proposed algorithms.

3.1 SINGLE-PHASE SRF-PLL STRUCTURE

The block diagram of the conventional single-phase SRF-PLL is depicted in Figure 3.2. This structure is a closed loop feedback control system with a Proportional-Integral (PI) compensator. The single-phase input signal is transformed
into the virtual synchronous reference frame by using a Quadrature Signal Generator (QSG) and with the measured frequency and angle by the PLL. The error which is the \( q \) component output is then regulated to zero by the control system. It will be shown that the \( q \) component has a direct relationship with the phase of input signal. This means that with zero steady-state error, the calculated angle and frequency by PLL is equal to those of input signal, and PLL is locked and follows the angle and frequency of the input voltage. In addition, this structure can detect the frequency of input signal, if it is variable. The integration of the frequency value by the final integrator gives the value of signal voltage angle.

In order to generate the virtual quadrature component in the stationary reference frame, \( v_{β'} \), form a single-phase input voltage, \( v_i \), a 90° phase lag is applied to the signal. Therefore,

\[
V_i = V_1 \cos(\omega_1 t + \phi_1) \rightarrow V_{β'} = V_1 \sin(\omega_1 t + \phi_1)
\]  

After making the quadrature component, the signal is transformed to the synchronous reference frame by using (3.2).

\[
\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos \theta_o & \sin \theta_o \\ -\sin \theta_o & \cos \theta_o \end{bmatrix} \begin{bmatrix} v_{α'} \end{bmatrix}
\]  

In a steady and locked state, \( \theta_o \) equals to \( \omega_1 t + \phi_1 \). It is the calculated signal voltage angle which is fed back from PLL output. In the case of a distorted input signal, when only odd harmonics of the fundamental frequency are present, the \( q \) component which is supposed to be zero in a steady state contains some even harmonics as shown in (3.3).

\[
v_q(t) = V_2 \sin(2\omega_1 t + \phi_2) + V_4 \sin(4\omega_1 t + \phi_4) + \cdots
\]
The odd harmonics are the dominant harmonic content of power system voltage signals. The adverse effect of the distortion on the PLL outputs is generated even numbered harmonic ripples added to the detected angle and frequency. Therefore, in order to keep only the DC value, all the frequency content of \( v_q \) must be eliminated. A Moving Average Filter (MAF) can eliminate all the harmonic content of \( v_q(t) \) and keep the DC content, in a steady state. Its function is given as,

\[
\overline{v_q(t)} = \frac{1}{T_w} \int_{t-T_w}^{t} v_q(\tau) d\tau ,
\]

(3.4)

where \( T_w \) is the length of averaging window. MAF is a notch filter with zero gain at a fundamental frequency and the repeated integral multiples of that frequency. It operates by calculating the average of \( v_q \) over a window with the length of \( T_w \). If \( T_w \) is equal to the period of the fundamental frequency content of \( v_q \) which is \( 2\omega_1 \), as given in (3.3), this frequency content and the entire frequency content with frequencies equal to integral multiples of \( 2\omega_1 \) are averaged and removed. Thus, the proper value for \( T_w \) is given in (3.5). The MAF is effective in elimination of these frequencies up to the Nyquist frequency.

\[
T_w = \frac{\pi}{\omega_1}
\]

(3.5)

However, the frequency content of \( v_q \) which is generated by switching ripples and even numbered harmonics of the input signal is not always an integral multiple of \( 2\omega_1 \) and cannot be eliminated completely. Nonetheless, MAF and QSG have generally a limited bandwidth and can attenuate these high frequencies significantly.

Additionally, in transients, there may be large variations in the measured \( \omega \) caused by closed loop operation of PLL in following large phase and frequency variations. Since this frequency is used for adaptation of window length to frequency variations, a limiter is used to restrict the range of output frequency to \( \pm 0.1\omega_0 \), where \( \omega_0 \) is the centre frequency of PLL and is equal to \( 2\pi \times 50 \text{ rad/s} \). Therefore, the window length will remain limited which, as discussed in Section 3.4, is a necessity for digital realisation of MAF. In addition, low pass filtering of \( \omega \) is necessary for limiting its high frequency fluctuations which have adverse effects on the operation of QSG and may prevent the PLL from locking. Consequently, a first order Low Pass Filter (LPF) with a low bandwidth is used.
The modified structure for PLL is illustrated in Figure 3.2 in which a feedforward or a predictor compensator can be used to improve the performance of the system.

![Figure 3.2 Block diagram of modified single-phase SRF-PLL](image)

### 3.2 MODELLING OF PLL

For design of a proper controller for the feedback control system, the small-signal model of the PLL needs to be obtained. Therefore, the SRF transformation stage and MAF are modelled as follows.

#### 3.2.1 SRF Transformation Stage

The first stage of PLL consists of the QSG and the SRF transformation part. The small-signal model of this stage as obtained in this section will show that it is in fact a phase differentiator providing the difference between the input signal phase angle and the PLL output phase angle. Since the QSG is a phase shift filter with a limited bandwidth, it introduces a delay in the transformation. In order to obtain the model for this stage, the time response to a small-signal step phase change of input in a steady and locked state is calculated. Then, the transfer function is obtained by Laplace transform of the time response. For this application, two SRF transformation methods which use All Pass Filter (APF) and Second Order Generalised Integrator (SOGI) QSGs are discussed and modelled.

**SRF Transformation by APF-QSG**

The quadrature component can be made by an APF with the following transfer function.

$$G_{APF}(s) = \frac{\omega_0 - s}{\omega_0 + s}, \quad (3.6)$$

where $\omega_0$ is the centre frequency of the filter. The frequency response of this filter has a unity gain with an infinite bandwidth. It also introduces a $90^\circ$ phase lag at $\omega$ in
order to generate the $\beta'$ component. APF is a simple method which can be implemented with low amount of computations.

For modelling purpose, a sinusoidal input signal with $\phi_1 = 0$ in a steady state is considered. Then, a small phase step change, $\delta \phi_1$, at $t = 0$ is introduced in the signal. By using the small-signal approximation for $\delta \phi_1$, (3.7) is obtained.

$$v'_{\alpha}(t) = v_{i}(t) = V_1 \cos(\omega ft) + V_1 \left[ \cos(\omega ft + \delta \phi) - \cos(\omega ft) \right] u(t) \approx V_1 \cos(\omega ft) - \delta \phi V_1 \sin(\omega ft) u(t).$$

(3.7)

The time response of $v'_{\beta'}$ is calculated by finding the time response of APF to $v'_{\alpha'}$ with the assumption of $\omega_1 = \omega_0$, as given in (3.8).

$$v'_{\beta'}(t) \approx V_1 \sin(\omega f t) - \delta \phi V_1 \frac{\omega_0 - s}{s^2 + \omega_0^2} \omega_0 + s] = V_1 \sin(\omega f t) + \delta \phi V_1 \left[ \cos(\omega f t) - e^{-\omega f t} \right] u(t)$$

(3.8)

$v_q$ is then obtained using SRF transformation in (3.2).

$$v_q(t) \approx \delta \phi V_1 \left[ 1 - \cos(\omega f t) e^{-\omega f t} \right] u(t)$$

(3.9)

The second order transfer function of the transformation stage is obtained by calculating the Laplace transform of (3.9) and eliminating the Laplace of the assumed step input, $\Delta \phi_1 / s$. Gain of the transfer function is dependent on the amplitude of the signal, but it has been considered as unity in the following equations for simplicity of representation. The transfer function is given in (3.10). It can also be approximated with a first order filter by using MATLAB order reduction for simplifying the transfer function.

$$G_{APF}^{SRF}(s) = \frac{V_q(s)}{\Delta \phi_1(s)} = -\frac{\omega_0 (s + 2\omega_0)}{s^2 + 2\omega_0 s + 2\omega_0^2} \approx \frac{2\omega_0}{s + 2\omega_0}$$

(3.10)

By following a similar approach, the transfer function of the transformation stage to small-signal frequency variations, $\Delta \omega_1$, is obtained as given in (3.11).

$$G_{SRF, \omega}^{APF}(s) = \frac{V_q(s)}{\Delta \omega_1(s)} = -\frac{1}{2\omega_0} \cdot G_{SRF}^{APF}(s) = G_{\omega} G_{SRF}^{APF}(s)$$

(3.11)
**SRF Transformation by SOGI-QSG**

SOGI is a type of filter structure based on the Generalised Integrator (GI) [16]. The structure is presented in Figure 3.3.

![Figure 3.3 Block diagram of SOGI-QSG](image)

Compared to APF, SOGI needs a few more computations, but it has the benefit of filtering. It can attenuate all the harmonic content apart from the fundamental frequency content in both the $v_{\alpha'}$ and $v_{\beta'}$ components. This extra filtering may improve the transients, because of the adverse effect of harmonics entered in the control loop and the slow dynamics of MAF in removing them. It also attenuates the frequency content that cannot be eliminated by MAF. They include even numbered harmonics and switching harmonics which are not integral multiples of the fundamental frequency. One other aspect of SOGI is the ability to implement an FLL as will be discussed in Section 3.6. The transfer functions of SOGI are given in (3.12) and (3.13).

\[
H_{\alpha'}(s) = \frac{V_{\alpha'}(s)}{V_i(s)} = \frac{k \omega_0 s}{s^2 + k \omega_0 s + \omega_0^2}, \quad (3.12)
\]

\[
H_{\beta'}(s) = \frac{V_{\beta'}(s)}{V_i(s)} = \frac{k \omega_0^2}{s^2 + k \omega_0 s + \omega_0^2}, \quad (3.13)
\]

where $k$ is the damping factor, and $\omega_0$ is the centre frequency of SOGI. From the transfer functions, it is concluded that at $\omega_0$, $v_{\beta'}$ is 90° lagged from the input signal, and $v_{\alpha'}$ is in phase with the input. The damping factor $k$ defines the bandwidth of the filter. The Bode plots for different values of $k$ are illustrated in Figure 3.4. The lower values of $k$ lead to less damped but more filtered outputs. However, filtering can reduce the speed of the SRF transformation and also makes the phase shift in frequency response more susceptible to frequency variations.
The small-signal model for the SRF transformation stage with SOGI is obtained by following the similar approach as before and with the assumption of $V_1 = 1$. First, the time response of $v_q(t)$ to a step phase change is calculated, as given in (3.14).

\[
\begin{align*}
\dot{v}_q(t) &= \delta \phi_k \\
\delta \phi &= -\frac{k}{\sqrt{4-k^2}} \left( \sin \left( (K+1)\omega f \right) - \sin \left( (K-1)\omega f \right) \right) + \\
&\quad + \left( \left( 1 - \frac{1}{K} \right) \cos \left( (K+1)\omega f \right) + \left( 1 + \frac{1}{K} \right) \cos \left( (K-1)\omega f \right) \right),
\end{align*}
\]

(3.14)

where,

\[
K = \sqrt{1 + \frac{k^2}{4}}, \quad 0 \leq k < 2.
\]

(3.15)
Then, the transfer function is obtained as given in (3.16). The transfer function can also be approximated with a first order filter by using MATLAB order reduction for simplification of the transfer function.

\[
G_{SRF}^{SOGI}(s) = \frac{V_q(s)}{\Delta \phi_1(s)} = \frac{k \omega_b^3 (2s + k \omega_b)}{s^4 + 2k \omega_b s^3 + (4 + k^2) \omega_b^3 s^2 + 4k \omega_b^3 s + k^2 \omega_b^4} \approx \frac{k \omega_b/2}{s + k \omega_b/2} \quad (3.16)
\]

The transfer function of the transformation stage to small-signal frequency variations is also obtained as given in (3.17).

\[
G_{SRF,\omega}^{SOGI}(s) = \frac{V_q(s)}{\Delta \omega_1(s)} = -\frac{2}{k \omega_b} \cdot G_{SRF}^{SOGI}(s) = G_{\phi} G_{SRF}^{SOGI}(s) \quad (3.17)
\]

The time response data of the SRF transformation stage with the two discussed QSG filters and with the centre frequency of 50 Hz are summarised in Table 3.1. The best settling time is achieved with \(k = 1.41\).

<table>
<thead>
<tr>
<th>QSG</th>
<th>Settling time (ms)</th>
<th>Rise time (ms)</th>
<th>Overshoot (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>APF</td>
<td>11.9</td>
<td>3.6</td>
<td>6.7</td>
</tr>
<tr>
<td>SOGI</td>
<td>k = 0.35</td>
<td>67.9</td>
<td>39.5</td>
</tr>
<tr>
<td></td>
<td>k = 0.70</td>
<td>34</td>
<td>15.1</td>
</tr>
<tr>
<td></td>
<td>k = 1.00</td>
<td>18.1</td>
<td>12.2</td>
</tr>
<tr>
<td></td>
<td>k = 1.41</td>
<td>8.2</td>
<td>5.0</td>
</tr>
<tr>
<td></td>
<td>k = 1.99</td>
<td>16</td>
<td>4.2</td>
</tr>
</tbody>
</table>

3.2.2 Moving Average Filter (MAF)

The transfer function of the MAF is obtained by calculating the Laplace transform of MAF function in (3.4), as given in (3.18).

\[
G_{MAF}(s) = \frac{V_q(s)}{V_q(s)} = \frac{1 - e^{-T_w s}}{T_w s} \quad (3.18)
\]

In order to obtain the frequency response, \(s\) is substituted with \(j \omega\).

\[
G_{MAF}(j \omega) = \left| \frac{\sin(\omega T_w/2)}{\omega T_w/2} \right| - \frac{\omega T_w}{2} \quad (3.19)
\]
It shows that MAF has zero gain at frequencies equal to integral multiples of $1/T_w$, and consequently, they are eliminated at the output. As explained in Section 3.1, for elimination of odd numbered harmonic content of $v_q$ which are introduced by a distorted 50 Hz signal, a window length of equal to 10 ms is required.

The transfer function in (3.18) can be approximated by using the first order Padé approximation of time delay function [26], as given in (3.20).

$$G_{MAF}^{approx}(s) = e^{-T_w s} = \frac{1 - s T_w / 2}{1 + s T_w / 2} \approx \frac{2/T_w}{s + 2/T_w}$$

(3.20)

MAF can also be approximated for low frequencies by a time delay equal to half a window length, as given in (3.21).

$$G_{MAF, \text{delay}}^{approx}(s) = e^{-T_w / 2 s} \approx 1 - \frac{T_w / 2 s}{2 s} e^{-T_w / 2 s}$$

(3.21)

Bode diagram in Figure 3.5 shows the frequency response of MAF and its first order approximation. The magnitude of the approximated transfer function is the envelope of that of MAF. This approximation is used for simplification of the control design.

Figure 3.5 Bode plot of MAF (red) and the approximated transfer function (blue)
The obtained small-signal model in the phase domain is presented in Figure 3.6. It contains both the frequency and phase loops. The direct relationship of the loop gains to the amplitude of the input signal, $V_1$, is also included in the model. Design of the controller and the compensator is described as follows.

**3.3 DESIGN OF CONTROLLER**

As was shown in the previous section, transfer function of MAF can be approximated by a first order filter with a slow pole at $s = -2/T_w$. This introduces a phase lag into the control loop and also limits its bandwidth. The phase lag may reduce the stability margins, and the limited bandwidth reduces the response speed of the PLL. The PI compensator cannot effectively compensate the adverse effects of MAF. Therefore, the performance of MAF must be compensated by a proper compensation method in order to achieve a satisfactory PLL performance. A few methods have been proposed for speeding up the system. Lead compensator and delay compensation predictor can be used to replace the slow pole with a faster one. These compensators as well as the introduced feedforward compensator are described in the following sections.

### 3.3.1 Lead Compensator and Delay Compensation Predictor

The transfer function of an appropriate lead compensator for the compensation of MAF is given in (3.22) [26].

$$G_{comp}^{lead}(s) = \frac{1 + sT_w/2}{1 + s/\omega_{p,lead}}, \quad \omega_{p,lead} \gg \frac{2}{T_w} \quad (3.22)$$

It introduces a zero into the control loop on real axis at $s = -2/T_w$ which cancels out the approximated pole of MAF. It also has a real pole with a value much greater than the zero. In other words, the lead compensator shifts the slow pole to the left on the real axis and increases the open loop bandwidth and compensates the phase lag.
Delay compensation predictor is designed based on the linear prediction of the MAF output. As was shown in (3.21), MAF can be approximated by a delay equal to $T_w/2$. The discrete-time function in (3.23) linearly predicts the MAF output for the length of this delay. It is performed by calculation of the slope of the filter output with the two most recent output values [24].

$$v_g^{\text{pred}}[k] = v_g[k] + \frac{T_w}{T_s} (v_g[k] - v_g[k-1])$$  \hspace{1cm} (3.23)

This equation shows that the prediction algorithm is dependent on the window length, $T_w$. Therefore, for a better compensation in case of a variable frequency input, it could be adapted to the window length. The z-transform in (3.24) shows that the transfer function has a phase lead which compensates the phase lag of MAF.

$$G_{\text{comp. pred.}}(z) = \left( \frac{T_w}{2T_s} + 1 \right) - \frac{T_w}{2T_s} z^{-1} \xrightarrow{\text{Backward Euler}} 1 + sT_w/2$$  \hspace{1cm} (3.24)

Converting the transfer function to continuous-time domain by using backward Euler method shows that this transfer function is equivalent to a single zero at $s = -2/T_w$. Thus, the predictor is equivalent to the lead compensator with a pole at infinity. Therefore, it is not much more effective in speeding up the system than the lead compensator because of other slow poles in the control loop which limit the bandwidth and the phase lag compensation of the system. The predictor and the PI controller in series work as a PID controller with the following transfer function.

$$G_{\text{comp.}} G_c = \left( K_p + \frac{K_i T_w}{2} \right) + \frac{K_i}{s} + \frac{K_p T_w}{2s}$$  \hspace{1cm} (3.25)

### 3.3.2 Feedforward Compensator

Feedforward is another method which can be used for delay compensation of the MAF. It introduces a zero in the open loop transfer function which adds a phase lead to the frequency response. Thus, it can compensate the phase lag of the slow pole of the MAF. Feedforward can also improve the performance for large phase variations of the input signal. When there is a large change in the input phase, early estimation of the phase change by a feedforward compensator improves the speed of system in response to the large phase variations.
The feedforward link was illustrated in the Figure 3.2. By using the averaged values of \( v_d \) and \( v_q \) as shown in (3.26), an estimation of the \( \Delta \phi_1 \) can be obtained.

\[
\phi_{FF} = \arctan \left( \frac{v_q}{v_d} \right)
\]

(3.26)

This value is added to the output angle before the PI compensator and the closed loop control system can respond to the phase variations. In a steady state, the average value of \( v_q \) converges to zero and so does the \( \phi_{FF} \). The feedforward term must be calculated by using the averaged \( v_d \) and \( v_q \) values in order not to include their harmonic ripples. For large-signal variations, \( v_q \) is smaller than and not linearly related to the \( \Delta \phi_1 \). However, the term in (3.26) results in a linear relationship between the \( \phi_{FF} \) and \( \Delta \phi_1 \) which improves the performance of large-signal transients.

For realisation purpose, in order to reduce the time required for computation or table lookup of (3.26), this function is replaced with its derivative as,

\[
\dot{\phi}_{FF} = \frac{v_q v_d - v_d v_q}{(v_q)^2 + (v_d)^2} \approx \frac{v_{q0}}{v_d} v_q.
\]

(3.27)

This value is added to the input of the PLL final integrator to be integrated as \( \phi_{FF} \) in the output as was shown in Figure 3.2. The small-signal approximation of this term in (3.27) shows that it acts as a derivative term with the above mentioned advantages. This derivative controller is added to the PI controller. Therefore, another degree of freedom is added to the control design by feedforward coefficient, \( K_{FF} \).

Since the average of \( v_d \) is also required in this method, another MAF needs to be implemented. However, it doubles the amount of memory required for digital realisation of PLL algorithm. Nonetheless, if a normalisation algorithm for amplitude of the input signal is required, the averaged value of \( v_d \) which is in direct relationship with the amplitude of the input signal must be obtained. In addition, the locked state of PLL can also be detected by comparing the averaged \( v_d \) with a threshold value. Therefore, this extra MAF is required for other purposes as well.

### 3.3.3 Controller Tuning

The open and closed loop transfer functions of the PLL system are calculated in (3.28) and (3.29).
\begin{align*}
G_{OL}(s) &= V_1 G_{MAF} G_{comp} G_c \left( \frac{1}{s} + G_{SRF} G_{LPF} G_\omega \right), \\
G_{CL}(s) &= \frac{V G_{SRF} G_{MAF} G_{comp} G_c}{s (1 + G_{OL})},
\end{align*} 
(3.28) \tag{3.28} \\
(3.29) \tag{3.29}

where,
\begin{equation}
G_c = \left[ K_{FFS} + K_p + \frac{K_i}{s} \right].
\end{equation} \tag{3.30} 

It is observed that the loop gain depends on the amplitude of the input signal, \( V_1 \). This makes the control performance sensitive to amplitude variations. An adaptive method can be implemented in order to make the loop gain independent of the input voltage amplitude. However, the amplitude variations of the grid voltage are limited and its effect on the control performance is very small. Therefore, the input signal is normalised to unity and the approximation of \( V_1 = 1 \) is used.

The controller is tuned in the continuous-time domain. However, if the gain crossover frequency, \( \omega_{crossover} \), and the sampling interval, \( T_s \), satisfy the inequality of (3.31), the discretised system will have a satisfactory performance [104].
\begin{equation}
\omega_{crossover} < \frac{\pi}{5T_s},
\end{equation} \tag{3.31} 

The different compensators including PI, PI-Predictor and PI-Feedforward controllers are tuned and their performances are compared. For the purpose of PID tuning, MATLAB PID Tuner is used. The objective of tuning is to minimise the settling time and rise time while satisfying a minimum of 45° phase margin and 8 dB gain margin. The margins are required in order not to allow the modelling approximations, and variations in the system dynamics because of nonlinearities caused by large-signal variations affect the stability of the system.

The results are summarised in Table 3.2 which shows the step response and frequency response data with different compensators and different QSGs. Tuning was done for different values of damping factor, \( k \), for SOGI in order to compare the performance. It can be observed that the feedforward and the predictor compensator have similar small-signal responses and have been able to improve the response speed, overshoot and stability margins of the system. The table also shows that the PLL with SOGI-QSG and with higher damping factor has faster response compared
to the APF-QSG. It is worth noting that MAF eliminates the effect of odd harmonics of the input signal. However, the weak even numbered and switching harmonics are only attenuated by MAF, and extra attenuation by SOGI helps in reducing their ripples at the output. Therefore, in order to have a balance between filtering and performance, the SOGI-QSG with the damping factor of $k = 1.41$ is chosen for the implementation of the PLL. Figure 3.7 shows Bode plots of the open loop transfer function as well as the step response with the PI-FF controller.

Table 3.2 Control design results including time response and frequency response data for different control structures

<table>
<thead>
<tr>
<th>Quadrature signal generator</th>
<th>Settling time, Rise time, Overshoot</th>
<th>Gain margin, Phase margin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$f_{LPF}$</td>
<td>$K_p$, $K_i$</td>
</tr>
<tr>
<td></td>
<td>PI</td>
<td>PI-Pred.</td>
</tr>
<tr>
<td>APF</td>
<td>67 ms, 10 ms, 44%</td>
<td>53 ms, 6.1 ms, 35%</td>
</tr>
<tr>
<td></td>
<td>14 dB, 41°</td>
<td>18 dB, 62°</td>
</tr>
<tr>
<td></td>
<td>5.3 Hz</td>
<td>18.2 Hz</td>
</tr>
<tr>
<td></td>
<td>91.4, 3477</td>
<td>206.9, 9129</td>
</tr>
<tr>
<td>SOGI $k=0.70$</td>
<td>121 ms, 17 ms, 39%</td>
<td>65 ms, 7.7 ms, 35%</td>
</tr>
<tr>
<td></td>
<td>17 dB, 52°</td>
<td>12 dB, 49°</td>
</tr>
<tr>
<td></td>
<td>3 Hz</td>
<td>7 Hz</td>
</tr>
<tr>
<td></td>
<td>71.8, 1897</td>
<td>267.4, 24440</td>
</tr>
<tr>
<td>SOGI $k=1.00$</td>
<td>97 ms, 13 ms, 42%</td>
<td>54 ms, 6.6 ms, 39%</td>
</tr>
<tr>
<td></td>
<td>15 dB, 48°</td>
<td>12 dB, 53°</td>
</tr>
<tr>
<td></td>
<td>3.6 Hz</td>
<td>7.4 Hz</td>
</tr>
<tr>
<td></td>
<td>83.3, 2569</td>
<td>245.6, 22200</td>
</tr>
<tr>
<td>SOGI $k=1.41$</td>
<td>76 ms, 11 ms, 48%</td>
<td>46 ms, 5.9 ms, 45%</td>
</tr>
<tr>
<td></td>
<td>14 dB, 44°</td>
<td>12 dB, 57°</td>
</tr>
<tr>
<td></td>
<td>4.3 Hz</td>
<td>8.2 Hz</td>
</tr>
<tr>
<td></td>
<td>96.6, 4356</td>
<td>232.9, 20890</td>
</tr>
<tr>
<td>SOGI $k=1.99$</td>
<td>60 ms, 8.7 ms, 55%</td>
<td>39 ms, 5.5 ms, 59%</td>
</tr>
<tr>
<td></td>
<td>13 dB, 39°</td>
<td>12 dB, 58°</td>
</tr>
<tr>
<td></td>
<td>4.7 Hz</td>
<td>8.8 Hz</td>
</tr>
<tr>
<td></td>
<td>111, 4564</td>
<td>223.7, 19930</td>
</tr>
</tbody>
</table>
For digital realisation of PLL algorithm, discretisation of the continuous-time components is required. The input signal is sampled with a sampling rate of $f_s$ equal to 30 kHz. In a steady state as given in (3.32) and illustrated in Figure 3.8, the calculated output angle in each sampling interval, $\theta_o[k]$, is equal to the angle of the signal at the next sampling step, $k+1$, because of the uncompensated one sampling interval loop delay of PLL as well as the small sampling interval. This value is used at the next sampling step as the angle feedback value for the SRF transformation stage. It must be noted that because of the low bandwidth of PLL, this small loop delay does not affect the stability of the control system.
Discretisation of components is described as follows. The discrete equivalent of APF is given in (3.33).

\[ G_{APF}(z) = \frac{z^{-1}e^{-\omega_0 T_s}}{1 - e^{-\omega_0 T_s}z^{-1}} \]  

(3.33)

It can be realised by using Direct Form II (DF-II) for digital filter realisation as shown in Figure 3.9. The exponential term can be approximated by the first few terms of its Taylor series for reducing the amount of computations. Taylor series in (3.34) with the first four terms gives full word-length accuracy with single-precision floating point realisation for the limited variation range of \( \omega_0 T_s \).

\[ e^{-\omega_0 T_s} \approx 1 - \omega_0 T_s + \omega_0^2 T_s^2 / 2 - \omega_0^3 T_s^3 / 6 \]  

(3.34)

The integrators are discretised by using Tustin method [104] as given in (3.35). First order filters are not sensitive to round-off error and can be realised in Direct Form I (DF-I) [105].

\[ \frac{1}{s} \rightarrow \frac{T_s}{2} \cdot \frac{1 + z^{-1}}{1 - z^{-1}} \]  

(3.35)
SOGI is also discretised by using Tustin method, as given in (3.36) and (3.37).

\[
H_{\alpha}(z) = \frac{b_0 \left[1 - z^{-2}\right]}{a_0 + a_1 z^{-1} + a_2 z^{-2}} = \frac{2k \omega_o T_s \left[1 - z^{-2}\right] \left[4 + (\omega_o T_s)^2 + 2k \omega_o T_s\right] + \left[2(\omega_o T_s)^2 - 8\right] z^{-1}}{\left[4 + (\omega_o T_s)^2 - 2k \omega_o T_s\right] z^{-2}}
\]

(3.36)

\[
H_{\beta}(z) = \frac{0.5 \omega_o T_s b_0 \left[1 + 2z^{-1} + z^{-2}\right]}{a_0 + a_1 z^{-1} + a_2 z^{-2}}
\]

(3.37)

SOGI can be realised in DF-II as illustrated in Figure 3.10.

The LPF with the cut-off frequency of \(\omega_c\) is discretised by using the forward Euler method as given in (3.38). The forward Euler method cannot always preserve the stability, and it may generate an unstable discretised system [104]. However, the discretised transfer function shows that the pole is always inside the unity circle and the stability is preserved.

\[
G_{LPF}(z) = \frac{T_0 \omega_c z^{-1}}{(1 + T_0 \omega_c) - z^{-1}}
\]

(3.38)

The derivative terms in the feedforward function in (3.27) are discretised by using the backward Euler method. By using this method, the discrete-time equivalent of this function will be simplified to (3.39) where \(k\) is the current sampling step.

\[
\dot{\theta}_{FF}[k] = \frac{1}{T_s} \frac{v_q[k] v_d[k] - v_d[k - 1] - v_d[k] v_q[k - 1]}{v_d[k] v_d[k] + v_q[k] v_q[k]}
\]

(3.39)
Compared to the predictor compensator, perform of a division is also required. This adds to the computation time. However, by using a fast optimised floating point division method, the execution time is reduced to 24 CPU cycles of the employed digital controller which is also faster compared to 53 cycles for the $\tan^{-1}$ function [106].

The discrete MAF function is given in (3.40) which can be implied by considering the equivalent of continuous-time MAF function of (3.4) in discrete-time domain. The function can be simplified as shown in the same equation in order to make it suitable for digital realisation.

\[ \bar{v}_q[k] = \frac{1}{N} \sum_{i=k-N+1}^{k} v_q[i] \]
\[ = v_q[k-1] + \frac{1}{N} (v_q[k] - v_q[k-N]), \]  
\text{(3.40)}

where,

\[ N = \frac{T_w}{T_s}. \]  
\text{(3.41)}

The discrete-time transfer function of MAF is obtained by $z$-transform of (3.40) as given in (3.42).

\[ G_{MAF}(z) = \frac{1 - z^{-N}}{N (1 - z^{-1})}. \]  
\text{(3.42)}

This filter needs some memory of the digital controller as a circular array in order to store the previous sampled values of the MAF input for the period of its window length. It means that for the window length of $T_w$ and the sampling interval of $T_s$, storage of $(N+1)$ previous sample values is required. For example, the output frequency of PLL is limited to between $\pm0.1\omega_0$, i.e. 45 and 55 Hz, and therefore, the maximum window length is 11.1 ms, and with the 30 kHz sampling rate, the storage of 334 consecutive sampled values of the MAF input is required.

If this filter is realised via DF-II, the signal is first passed through an all-pole filter which has a marginally stable pole at $z=1$. This all-pole filter works as an accumulator for all the previous input values, and therefore, the accumulated value may overflow in a fixed point implementation or may become inaccurate because of
round-off error in a floating point implementation. Therefore, DF-I is used for realisation of MAF instead of DF-II, as shown in Figure 3.11.

![DF-I realisation of MAF](image)

**Figure 3.11 DF-I realisation of MAF**

### 3.5 FREQUENCY ADAPTIVE MOVING AVERAGE FILTER

The fundamental frequency of the grid voltage is not constant. Therefore, in order to be able to eliminate the harmonic ripples, the length of the averaging window must dynamically change according to the detected frequency by PLL. A problem of the discrete MAF is that $T_w$ must be exactly equal to an integral multiple of $T_s$, otherwise the output of MAF will not be an accurate averaged value, and the effectiveness of MAF in eliminating harmonic ripples degrades. In order to improve the averaging some methods have been proposed.

One method is to define $N$ equal to the nearest integer by using Round function [30]. The accuracy of this method is dependent on the sampling interval. Oversampling can be used in order to decrease the sampling interval and therefore increase the resolution of the averaging window. However, sampling rate of Analogue to Digital Converters (ADC), processor speed and available memory of digital controller may limit the oversampling rate. The amount of required memory is multiplied by the rate of oversampling.

Another method is the variable sampling rate in which the sampling interval is adjusted according to the detected frequency so as to be an integer division of the detected period with a constant $N$ [34, 35]. This method is very effective, but its digital implementation may have some difficulties because of other program routines that use a fixed frequency sampling such as converter control algorithm. These two types of sampling need to be implemented simultaneously.

More practical methods include linear or polynomial approximation of the sample values between two consecutive samples [31]. The linear approximation method has been implemented and illustrated in Figure 3.12.
Equation (3.40) is corrected by addition of the integration over the partial sample value as given in (3.43) and (3.44), when the value of the measured frequency available at $k$-th sampling step is $\omega_o[k-1]$.

$$\bar{v}_q[k] = \frac{1}{N_f[k] + \alpha[k]} \left( v_q^{\text{sum}}[k] + v_q[k - N_f[k]] \cdot \alpha[k] \right), \quad (3.43)$$

$$v_q^{\text{sum}}[k] = v_q^{\text{sum}}[k - 1] + v_q[k] - v_q[k - N_f[k]], \quad (3.44)$$

where,

$$T_w[k] = \frac{\pi}{\omega_o[k-1]}, \quad (3.45)$$

$$N_f[k] = \text{Floor} \left( \frac{T_w[k]}{T_s} \right), \quad (3.46)$$

$$\alpha[k] = \frac{T_w[k]}{T_s} - N_f[k]. \quad (3.47)$$

$v_q^{\text{sum}}$ is the accumulator which contains the accumulated values of $v_q$ over the length of the averaging window. In order to reduce the computational load of CPU, the division term in (3.43) is replaced with $\omega_o[k-1]T_s/\pi$ which is the multiplication of the measured frequency by a constant value.

This algorithm is effective when the widow size variations are less than $\pm T_s$ and $N_f[k]$ remains constant, and therefore, the number of samples to be averaged by MAF is constant. This happens only for very limited frequency range or very low sampling rates. An algorithm for window resizing is required when the above conditions are not met. A resizing method is proposed in which the window length is shrunk or
expanded when the detected frequency is increasing or decreasing. When the window length needs expanding or shrinking, some extra samples are subtracted from or added to the accumulator of the MAF, and the averaging is updated over the new window length. Resizing of the window is implemented on a sample-by-sample basis which is described as follows.

A new variable is defined as $N_f[k]$. This variable stores the current window length defined by the algorithm. The initial value of this variable is set equal to the window length corresponding to the nominal centre frequency of PLL, $\omega_0$, as given in (3.48).

$$N_f[0] = N_f[0] = \text{Floor}\left(\frac{\pi}{T_s \omega_0}\right)$$

(3.48)

In every sampling step, $N_f[k]$ is calculated by using (3.45) and (3.46) based on the value of the detected frequency. If the value of $N_f$ is not changed, $N_f[k]$ is kept constant as well, and PLL works as normal. But, if the value of calculated $N_f[k]$ is different from the previous value of $N_f$, a one sample window resizing is performed. The algorithm is described in detail as follows and is depicted in Figure 3.13.

- **Expansion with new samples:**

  If the value of calculated $N_f[k]$ is greater than $N_f[k-1]$, the window is expanded by one sample, and $N_f[k]$ is increased by one. This indicates that the
window has been expanded by one sampling interval. Expansion is performed by addition of the most recent sample, \( v_q[k] \), to the MAF accumulator as it was done normally in (3.43). However, the value of the oldest sample, \( v_q[k - N_f' [k - 1]] \), remains in the accumulator and is not subtracted. This means that (3.49) and (3.50) need to be performed.

\[
\text{if } N_f[k] > N_f'[k - 1], \quad \text{then,} \\
N_f'[k] = N_f'[k - 1] + 1, \quad \text{and,} \\
v_q^{\text{sum.}}[k] = v_q^{\text{sum.}}[k - 1] + v_q[k],
\]

\[
\bar{v}_q[k] = \frac{1}{N_f'[k]} v_q^{\text{sum.}}[k]. \tag{3.50}
\]

- **Shrinkage with old samples:**

If the value of calculated \( N_f[k] \) is less than \( N_f'[k - 1] \), the window is shrunk by one sample, and \( N_f' \) is decreased by one. Shrinkage is performed by extra subtraction of an old sample, \( v_q[k - N_f'[k - 1] + 1] \), as well as the normal subtraction of \( v_q[k - N_f'[k - 1]] \) and normal addition of \( v_q[k] \). This means that (3.51) and (3.52) need to be performed.

\[
\text{if } N_f[k] < N_f'[k - 1], \quad \text{then,} \\
N_f'[k] = N_f'[k - 1] - 1, \quad \text{and} \\
v_q^{\text{sum.}}[k] = v_q^{\text{sum.}}[k - 1] + v_q[k] \\
- v_q[k - N_f'[k]] - v_q[k - N_f'[k - 1]],
\]

\[
\bar{v}_q[k] = \frac{1}{N_f'[k]} v_q^{\text{sum.}}[k]. \tag{3.52}
\]

The resizing continues as long as the calculated \( N_f[k] \) is not equal to \( N_f'[k - 1] \) which means that window length still needs to follow the frequency variations. When again, calculated \( N_f[k] \) becomes equal to \( N_f'[k - 1] \), it means that window length has settled to the new frequency, and MAF must operates normally with the new window length as was given in (3.43). With this algorithm, the MAF window length
follows the frequency variations sample by sample, and the operation of MAF in averaging does not deteriorate.

This algorithm needs only a few extra computations in every sampling step. It also has the advantage of a limited slew rate for window length resizing. This makes the window length variations less sensitive to the transient fluctuations of the $\omega_o$. In addition, the computational load of the employed CPU can be reduced by replacing the division terms in (3.50) and (3.52) by a multiplication terms equal to the already calculated $1/N_f^r[k]$. This is achievable by a lookup table stored in the memory, because $N_f^r[k]$ can only have a limited range of integer values. The table stores the already inversed values of $N_f^r$ for the limited frequency range of $\omega_o$.

Moreover, in order to improve the performance of the algorithm, the slew rate of the resizing can be further reduced in order to make it less sensitive to the transient fluctuations of the measured frequency introduced by phase variations. For this purpose, the condition for $N_f$ and $N_f^r$ is checked in every $m$-th sampling step rather than in every step, and window resizing is performed with the same rate. However, limiting the slew rate may reduce the response speed to frequency variations. Therefore, there must be a balance between the response speed to frequency variations and transient response of MAF resizing. By using (3.53) for limiting the slow rate to 2 Hz per main cycle, the value of $m$ is calculated to be 50 so that MAF resizing to a 2 Hz large frequency variation can be performed in a cycle of main frequency.

$$m = \frac{2f_0}{\text{Slew rate (Hz/cycle)}}$$  \hspace{1cm} (3.53)

### 3.6 SOGI-FLL WITH HARMONIC REJECTION

The Frequency-Locked Loop (FLL) is an effective structure for measuring the frequency and adapting the centre frequency of the SOGI. The FLL structure based on the SOGI filter, which was already illustrated in Figure 3.3, is depicted in Figure 3.14 [107].
In order to understand the behaviour of the FLL, the relationship between the
quadrature output signal, $v_{β'}$, and the error signal, $e_v$, should be considered. The
transfer function from the input signal, $v_i$, to the error signal is given by (3.54).

$$E_v(s) = \frac{s^2 + \omega^2}{s^2 + k \omega s + \omega^2}$$

(3.54)

In addition, the relationship between $v_i$ and $v_{β'}$, was already given in (3.13). Bode
diagrams of both $H_{β'}(s)$ and $E_v(s)$ are plotted in Figure 3.15.
It can be observed that when the frequency of input signal is lower than the SOGI resonant frequency \((\omega_i < \omega)\), the signals \(v_{\beta'}\) and \(e_v\) are in phase. But, when \(\omega_i > \omega\), they are in phase opposition. Therefore, a frequency error variable, \(e_f\), can be defined as the product of \(v_{\beta'}\) and \(e_v\). As shown in the Bode diagram, when \(\omega_i < \omega\), the average value of \(e_f\) is positive. When \(\omega_i = \omega\), it is zero, and when \(\omega_i > \omega\), it is negative. Therefore, an integral controller with a negative gain of \(-\gamma\) can be used to regulate the DC component of the frequency error to zero by shifting the SOGI resonant frequency, \(\omega\), until it becomes equal to the input frequency, \(\omega_i\) [16].

When odd numbered harmonics are present in the input signal, the result of multiplication term in a steady state when \(\omega_i = \omega\) is given in (3.55).

\[
\begin{align*}
\varepsilon_f &= \varepsilon_v v_{\beta'} = (v_i - v_{\alpha'}) \cdot v_{\beta'} \\
&= (V_3 \cos(3\omega t + \phi_3) - V_{3\alpha'} \cos(3\omega t + \phi_{3\alpha'}) + \cdots) \\
&\quad (V_1 \sin(\omega t + \phi_1) + V_{3\beta'} \sin(3\omega t + \phi_{3\beta'}) + \cdots) \\
&= V_0' + V_2' \sin(2\omega t + \phi_2') + V_4' \sin(4\omega t + \phi_4') + \cdots
\end{align*}
\]

Because harmonics are present in all the input and output signals, including \(v_i\), \(v_{\alpha'}\) and \(v_{\beta'}\), the steady-state frequency error is not zero and some even harmonics and a DC value exist in the output. The harmonics introduce some ripple into the detected frequency. In addition, the DC value, which is in relationship with the magnitude of the harmonic content, makes the FLL control loop shift the SOGI resonant frequency in order to regulate the error to zero. Therefore, a steady-state error is added to the detected frequency. This shows that SOGI-FLL does not have an error free output when its input contains harmonics. All the harmonic content must be detected and removed from the input signal [108]. If harmonics are detected selectively, only the selected harmonics can be removed from the input signal, and the steady-state error cannot be eliminated.

A new configuration is proposed which integrates both the PLL and FLL in order to be able to use the FLL with a distorted input signal. It works based on the idea that by removing the harmonic content from \(v_{\beta'}\), the DC value is removed from the multiplication result of (3.55), and only even numbered harmonic ripples will be present in the result. These harmonic ripples are eliminated by a MAF with an
adaptive window length in order to have a ripple free frequency output. The block diagram is depicted in Figure 3.16.

The fundamental content of $v_{\beta'}$ is reproduced by using the output angle obtained by PLL, and it is fed back to the SOGI-PLL. Compared to the conventional SRF-PLL, this configuration needs one more MAF as well as some extra computations for the FLL implementation. The predictor compensators are placed for both MAFs so as to improve the introduced phase lag by these filters into the frequency and phase loops.

### 3.7 PHASE MEASUREMENT FOR SELECTIVE HARMONICS

The harmonic compensation algorithm used by DVR needs to have information about the harmonic content of the grid voltage. This information includes the amplitude and the angle of the selected harmonic voltages. In the proposed method, these data is obtained by using a stacked PLL structure as illustrated in Figure 3.17 and discussed as follows. Each PLL is tuned in a selected harmonic frequency. The odd numbered harmonics are the significant harmonic contents of the voltages and currents in single-phase grids. Therefore, for the measurement of harmonic voltage angles up to the 7th order, four stages of PLL are used.

The first stage is in fact the previously designed SRF-PLL for the fundamental harmonic content. It measures the frequency and angle of the first harmonic voltage and rejects the other harmonic content. Since the harmonic frequencies are odd integral multiples of this frequency, the centre frequency for the SOGI in all other

Figure 3.16 Block diagram of integrated SOGI-FLL and SOGI-PLL for harmonic rejection
stages can be obtained from this stage. This means that the quadrature components of the selected harmonics are made by the corresponding SOGI at each stage.

In addition, these calculated centre frequencies can also be fed to the harmonic stages as the centre frequency feedforwards. However, since the integration of the frequency value is already being done in the first stage as the voltage angle, $\theta_1$, by the final integrator, the final integrators in the harmonic stages can be removed and the output angle from the first stage is multiplied by the harmonic orders and used as angle feedforwards for harmonic stages. Thus, in a steady state,

$$\theta_n^{FF}(t) = n \theta_1^{PLL}(t) = n (\omega t + \phi_1). \quad (3.56)$$

In addition, in the FLL structure in Figure 3.16, the $\omega t$ value can be used for this purpose.
The elimination of the phase integrators reduces the amount of computations required for the realisation of an extra final integrator for each stage. The closed loop operation in each harmonic stage now only needs to regulate its output phase, $\phi_n$, and compensate the phase value entered from the first stage, $n\phi_1$. This is done by the regulation of the compensation phase, $\phi_c^n$, as indicated in Figure 3.17 and given in (3.57).

$$\theta^n_n(t) = n\omega t + \phi_n = n\omega t + (n\phi_1 + \phi_c^n)$$  \hspace{1cm} (3.57)

In the harmonic stages as well as the first stage, some harmonic frequency content is entered in the $dq$ components. MAF filters can effectively eliminate this harmonic content in the harmonic stages as well. Equation (3.58) shows the harmonic content of the $q$ component for the harmonic stage tuned in the $n^{th}$ harmonic frequency.

$$v_q^n(t) = V_a \sin(\Delta \phi_n) + V_2 \sin(2\omega t + \phi_2) + V_4 \sin(4\omega t + \phi_4) + \cdots$$  \hspace{1cm} (3.58)

It can be observed that for harmonic stages, just like the first stage, only the even harmonics enter the control loop, and they must be eliminated. Therefore, for each stage, a MAF with the same length as the one for the fundamental stage must be implemented. These new MAFs must also be frequency adaptive. They all use the measured frequency of the first stage, $\omega_o$, and use the same adaptive algorithm. Thus, MAF window resizing for the first stage is applied to all other stages as well, and no extra effort for calculation of the window length is required. In addition, if the value of $1/N$ is not tabulated, it will be computationally time consuming as discussed in Section 3.5. Therefore, in this computationally effective algorithm, it needs to be calculated only once in every sampling interval and used in the computations for the MAFs in all the stages.

However, the extra MAFs consume some memory of the digital controller, and the available memory limits the number of MAFs which can be implemented. In order to reduce the memory usage of MAFs, sampling rate of the PLL can be reduced. Therefore, if the inverter control algorithm is implemented with a lower sampling rate, the value of the voltage angle in between the PLL sampling intervals can be interpolated by (3.59) for all the harmonics.
\[
\theta^n_o (kT_s + pT_s) = \left( \theta^n_o [k + 1] - \theta^n_o [k] \right) \times p + \theta^n_o [k]
\]
\[
= \left( \theta^n_o [k] - \theta^n_o [k - 1] \right) \times p + \theta^n_o [k - 1],
\]

(3.59)

where \(0 < p < 1\), and \(n\) is the harmonic order.

Another problem of this structure which is associated with the SOGI can be implied from the Bode plots of Figure 3.4. The \(\alpha'\beta'\) components are filtered at the frequencies above the centre frequency. However, the \(\beta'\) component is not well filtered at the frequencies below the centre frequency. Therefore, in each harmonic stage, the frequency content below the tuned frequency of that stage, which includes the lower order and fundamental harmonics, are not filtered effectively. The amplitudes of these contents, specially the fundamental content, are generally higher than the amplitude of the selected frequency of that stage. Despite the fact that ripples of this content are eliminated by MAF in a steady state, they enter the control loop during transients. Because of their high amplitudes compared to the selected harmonic amplitude, their interference has an adverse effect on the transient response of the stage and may even prevent the stage from locking to the harmonic voltage angle. Therefore, this lower frequency content must be removed from the input signal of each stage. For example, for the 5th harmonic stage, 3rd harmonic as well as the fundamental components are removed. Equation (3.60) shows how the input of \(n^{th}\) stage can be cleared from the lower order harmonic content.

\[
v_{i,n}^o(t) = v_i(t) - \sum_{m=1}^{n-2} V_m \cos(m \omega_{\alpha'} + \phi_m)
\]
\[
= v_i(t) - \sum_{m=1}^{n-2} V_m^d \cos(\theta_m^o(t)), \quad n = 1, 3, 5, 7
\]

(3.60)

The discrete-time domain realisation is given in (3.61)

\[
v_{i,n}^o[k] = v_i[k] - \sum_{m=1}^{n-2} V_m[k-1] \cos(\theta_m^o[k-1]), \quad n = 1, 3, 5, 7
\]

(3.61)

The subtracted terms in the equation are the regenerated harmonic content of the input signal \(v_i\). They are reproduced by using the angle and amplitude outputs of the PLL stages. Measurement of the amplitude of harmonics in a steady and locked state is obtained from the \(d\) component of the corresponding stage. This component is directly related to the input signal amplitude. Just like the \(q\) one, it also includes the
even numbered harmonic ripples which are eliminated by a MAF. The obtained amplitude is used for adaptation of the control loop to the harmonic voltage amplitude as discussed in the next section.

The advantage of this algorithm, compared to the previously presented ones in [21, 37] is that at each stage, the higher order harmonic content which are generally weaker and are already filtered by SOGI do not need to be eliminated from the input signal. They do not affect the transient performance considerably, and because of the presence of MAFs, their introduced ripples are removed in a steady state. In the previous methods, for having a ripple free and accurate output, all the harmonic contents which are not weak enough to have negligible effect on the output must be detected and removed at the input of each stage. This may require numerous PLL stages and is not computationally effective.

### 3.7.1 Adaptation to Amplitude of Harmonic Voltage

The loop transfer function for the each harmonic stage is given in (3.62). It shows that the loop gain has a direct relationship with the amplitude of the harmonic content. As opposed to the fundamental content, they have unknown amplitudes which could be small or large and variable. The controller for the stages is tuned for a normalised unity amplitude input signal. Therefore, if the amplitude of a harmonic is reduced, the loop gain decreases as well, and the response time to the phase and frequency variations as well as the steady-state error degrades. Therefore, the effect of the harmonic amplitude variations on the performance of the PLL stages cannot be neglected.

\[
G_{OE}^n(s) = V_n G_{MAF} G_{comp} \left[ K_p + \frac{K_i}{s} \right]
\]

As described in Section 3.7, \(\bar{V}_n^d\) has a direct relationship with the amplitude of the harmonic content at each stage, in a steady and locked state. This value is used to return the loop gain to normal. For this purpose, the quadrature output of the SRF transformation stage, \(v_q\), which is a part of the PLL loop is divided by the measured amplitude. Therefore, the dependency of the loop gain to the amplitude is eliminated. By using this algorithm, PLLs are able to measure the harmonic content as low as a few volts with negligible performance degradation. However, there are fluctuations in this value during transients which adversely affect the transient performance.
MAF provides some filtering, but a first order LPF with the bandwidth of 50 rad/s is also added to reduce the amount of transient fluctuations and improve the transient performance of the PLL harmonic stages.

Moreover, if the amplitudes of harmonics are small, during transients the measured amplitudes may temporarily become zero or negative. This affects the transient response of the stage. Therefore, $\bar{V}_n^d$ is limited to a minimum value in order to prevent a division by a very small value. This limit defines the minimum amplitude of harmonic for which the amplitude compensation can be performed effectively.

It can be observed from the loop transfer function in (3.62) that a compensator is also inserted in the control loop in order to compensate the MAF delay. The compensator for the harmonic stage is the predictor compensator of (3.23). Since the final integrators are omitted from the harmonic stages, and the feedforward compensator of (3.39) needs that integration, the predictor compensator is used instead. The results for controller tuning are summarised in Table 3.3. It shows that the control performance does not depend on the damping factor, as long as it is not small. For having a balance between filtering and performance, $k = 1$ is chosen.

<table>
<thead>
<tr>
<th>SOGI damping factor ($k$)</th>
<th>Settling time, Rise time, Overshoot</th>
<th>Gain margin, Phase margin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$K_p$, $K_i$</td>
<td>$K_p$, $K_i$</td>
</tr>
<tr>
<td></td>
<td>PI</td>
<td>PI-Pred.</td>
</tr>
<tr>
<td>0.70</td>
<td>27 ms, 14 ms, 0.5%</td>
<td>37 ms, 18 ms, 1%</td>
</tr>
<tr>
<td></td>
<td>11 dB, 52°</td>
<td>10 dB, 37°</td>
</tr>
<tr>
<td></td>
<td>0, 143</td>
<td>0, 392.9</td>
</tr>
<tr>
<td>1.00</td>
<td>35 ms, 11 ms, 9%</td>
<td>26 ms, 9 ms, 1%</td>
</tr>
<tr>
<td></td>
<td>11 dB, 51°</td>
<td>14 dB, 57°</td>
</tr>
<tr>
<td></td>
<td>0, 145.9</td>
<td>0, 260.6</td>
</tr>
<tr>
<td>1.41</td>
<td>37 ms, 11 ms, 13%</td>
<td>26 ms, 7.6 ms, 4%</td>
</tr>
<tr>
<td></td>
<td>12 dB, 56°</td>
<td>16 dB, 66°</td>
</tr>
<tr>
<td></td>
<td>0, 127.2</td>
<td>0, 218.1</td>
</tr>
<tr>
<td>1.99</td>
<td>36 ms, 10 ms, 15%</td>
<td>28 ms, 7 ms, 14%</td>
</tr>
<tr>
<td></td>
<td>12 dB, 58°</td>
<td>16 dB, 70°</td>
</tr>
<tr>
<td></td>
<td>0, 119.3</td>
<td>0, 198</td>
</tr>
</tbody>
</table>

The memory usage for implementation of this harmonic measurement algorithm is calculated to be equal to $(n_{max} + 1) \times (N_{max} + 1)$. $n_{max}$ is the maximum order of the
odd harmonics to be measured, and \(N_{\text{max}}\) is the maximum discrete length of the MAFs which is defined by the minimum measurable fundamental frequency of the first stage of PLL.

### 3.7.2 Improving the Accuracy of SRF Transformation

The discretised SOGI by Tustin approximation is not accurate, and there is a phase shift in the generated \(\alpha'\beta'\) components. This phase shift is larger for higher order harmonics, and therefore, it introduces a steady-state error into the output angle equal to the phase shift. With a small sampling interval of \(T_s\) the amount of error can be approximated for each stage with the centre frequency of \(n\omega_0\) as given in (3.63).

\[
e_{SOGI}^n \approx -\frac{(n\omega_0 T_s)^2}{6k} \text{ (rad)}, \tag{3.63}
\]

where \(k\) is the damping factor. Since the amount of error is known, it can be easily compensated at the output of each stage. However, for high sampling rates, the error is negligible. For example, for the 7\(^{th}\) harmonic, and \(k = 1.0\), it is about \(-5.13\times10^{-2}\)°.

In addition, more accurate \(\alpha'\beta'\) conversion can be achieved using the pre-warped Tustin approximation. By pre-warping the frequency \(s\), the frequency response of the discretised SOGI is exactly matched in both the magnitude and phase to the continuous-time one at a desired frequency, \(\omega^*\). The corrected Tustin approximation is given in (3.64) [104].

\[
s \rightarrow \frac{\omega^*}{\tan(\omega^* T_s/2)}, z^{-1} \frac{z - 1}{z + 1}, \tag{3.64}
\]

where \(\omega^*\) is the harmonic frequency for the corresponding discrete SOGI. The discretised SOGI transfer functions pre-warped for the \(n\)\(^{th}\)-order harmonic frequency are calculated as follows.

\[
H_{\alpha'} = \frac{k \sin(n\omega T_s)\left[1 - z^{-2}\right]}{\left[2 + k \sin(n\omega T_s)\right] - 4 \cos(n\omega T_s)z^{-1} + \left[2 - k \sin(n\omega T_s)\right]z^{-2}} \tag{3.65}
\]

\[
H_{\beta'} = \frac{k \left[1 - \cos(n\omega T_s)\right]\left[1 + 2z^{-1} + z^{-2}\right]}{\left[2 + k \sin(n\omega T_s)\right] - 4 \cos(n\omega T_s)z^{-1} + \left[2 - k \sin(n\omega T_s)\right]z^{-2}} \tag{3.66}
\]
3.8 SIMULATION STUDIES

Modelling and Simulation are performed in PSCAD/EMTDC. A highly distorted voltage with a normalised fundamental component, as plotted in Figure 3.18, is assumed as the input signal, $v_i$, for the PLLs in Figure 3.2 and Figure 3.17 as well as the FLL in Figure 3.16. It includes odd harmonics of 50 Hz from the $1^\text{st}$ to $11^\text{th}$ harmonics with the amplitude and phase listed in Table 3.4. The controller parameters for the PLL in Figure 3.2, $K_p$, $K_i$ and $K_{FF}$, are extracted from Table 3.2 with the damping factor of $k = 1.41$ for SOGI-QSG. In addition, the controller parameters for the harmonic measurement PLL in Figure 3.17 are extracted from Table 3.3 with the damping factor of $k = 1$ for SOGI-QSG.

![Figure 3.18 Input signal and its fundamental harmonic](image)

Table 3.4 Amplitude and phase of the harmonic content of the input signal

<table>
<thead>
<tr>
<th>Harmonic Order ($n$)</th>
<th>Normalised Amplitude</th>
<th>Phase Angle</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1^\text{st}$</td>
<td>1</td>
<td>0°</td>
</tr>
<tr>
<td>$3^\text{rd}$</td>
<td>0.417</td>
<td>120°</td>
</tr>
<tr>
<td>$5^\text{th}$</td>
<td>0.333</td>
<td>50°</td>
</tr>
<tr>
<td>$7^\text{th}$</td>
<td>0.250</td>
<td>105°</td>
</tr>
<tr>
<td>$9^\text{th}$</td>
<td>0.167</td>
<td>20°</td>
</tr>
<tr>
<td>$11^\text{th}$</td>
<td>0.125</td>
<td>0°</td>
</tr>
</tbody>
</table>

3.8.1 Case 1: Small-Signal and Frequency Measurement Performance

The first simulation case is plotted in Figure 3.19 which is the response of the fundamental harmonic stage to a small-signal $10^\circ$ step change in phase followed by a
2 Hz step change in the frequency of input signal, $v_i$, in order to show the performance of the designed PLL in Figure 3.2.

Figure 3.19 Response to a phase change at 300 ms followed by a frequency change at 400 ms, (a) measured phase, (b) frequency and (c) window length with PI-FF (blue) and PI-predictor (red)
Two types of compensators including feedforward and predictor are compared. The figures show that the measured phase angle, $\phi_o$, with both the compensators has been able to follow the phase variations, $\Delta \phi_i$, with zero steady-state error, and the responses are very similar. The measured frequency, $\omega_o$, has also been able to follow the frequency variations, $\Delta \omega_i$, with zero steady-state phase and frequency errors. The MAF window length, $N_f + \alpha$, also shows that it has followed the frequency variations in a slew rate limited manner. In addition, consistency with the step response of the model in Figure 3.7 shows the validity of the obtained model. However, the small difference is caused by the effect of harmonic contents and discretisation. For comparison, the phase response without any compensator is plotted in Figure 3.20. It shows that the compensators have been able to significantly improve the transient response of PLL with pure PI controller.

![Figure 3.20 Response with uncompensated PI controller to a small phase change at 300 ms followed by a frequency change at 450 ms, (a) measured phase and (b) measured frequency](image)

Figure 3.20 Response with uncompensated PI controller to a small phase change at 300 ms followed by a frequency change at 450 ms, (a) measured phase and (b) measured frequency
In addition, the response to the frequency change of 2 Hz, $\Delta \omega_i$, is also simulated without the adaptive window resizing. The results in Figure 3.21 shows that the phase angle and frequency outputs, $\phi_o$ and $\omega_o$, contain the harmonic ripples, and the steady-state errors do not settle to zero. Figure 3.22 shows the averaged $v_d$ and $v_d$ of the PI-Feedforward controller for this simulation case. The harmonics ripples are completely removed from these components which show the effectiveness of the adaptive window resizing during phase and frequency variations.

![Figure 3.21 Response to a frequency change without adaptive window resizing, (a) measured phase and (b) measured frequency with PI-FF (blue) and PI-predictor (red)](image-url)

Figure 3.21 Response to a frequency change without adaptive window resizing, (a) measured phase and (b) measured frequency with PI-FF (blue) and PI-predictor (red)
3.8.2 Case 2: Large-Signal Performance

Figure 3.23 shows the response of the PLL in Figure 3.2 to a 100° step change in the phase of input signal, $\Delta \theta_i$, as the second simulation case. The effect of feedforward compared to the predictor can be seen in the large-signal response. It has improved the rise time and overshoot compared to the predictor compensator. Settling time is about two main voltage cycles, and compared to the small-signal case, has no considerable increases.

During this large phase variation, large variations in the measured frequency, $\omega_o$, are expected, as plotted in Figure 3.23(b). However, the transient measured frequency is saturated by the frequency limiter of the PLL in Figure 3.2 such that the window length variations are limited. This is necessary for digital realisation of MAF, as discussed in Section 3.1 and 3.4.
Figure 3.23 Response to a large phase change, (a) measured phase and (b) measured frequency
3.8.3 Case 3: Small-Signal Harmonic Measurement Performance

For study of the PLL in Figure 3.17 for harmonic measurement, more cases were considered. In the third case, the response to a small phase change followed by a 2 Hz frequency change, $\Delta \phi_i$ and $\Delta \omega_i$, similar to the first case, is simulated. A step delay of 0.56 ms is entered into the input signal. It introduces $n \times 10^6$ phase change into the harmonic content. Figure 3.24 shows that the harmonic stage outputs, $\phi_{1,3,5,7}$, have been able to follow the phase variations, and they have been able to measure the normalised amplitudes, $\bar{V}_{1,3,5,7}$. The similar performance in the harmonic stages shows the effectiveness of the adaptation to amplitude of harmonics in maintaining the performance of PLLs regardless of the harmonic amplitudes.

![Figure 3.24 Response to a small delay at 300 ms followed by a 2 Hz frequency changes at 400 ms in the input signal, (a) measured phases and (b) measured amplitudes](image)
3.8.4 Case 4: Large-Signal Harmonic Measurement Performance

The fourth simulation case is plotted in Figure 3.25 with the same PLL and parameters as noted in the previous case. It is the response of harmonic stages to a large phase change. A step delay of 5.56 ms in the input signal introduces $n \times 100^\circ$ phase change into the harmonic contents. The results reveal that even during large phase variations, the harmonic stages have been able to measure the variations with no steady state error. The measured amplitudes are, however, fluctuating during the transient response. Nevertheless, their transient variations are not too high to considerably affect the PLL performance.

Figure 3.25 Response to large delay at 300 ms in the input signal, (a) measured phases and (b) measured amplitudes
3.8.5 Case 5 Harmonic Amplitude Measurement Performance

For the fifth case, a voltage sag equal to 25% of the nominal voltage is entered in the signal. Figure 3.26 shows that the harmonic stages measure the amplitude variations, and the measured phase angles are settled back to the harmonic phase angles. The measured amplitudes, $V_{1,3,5,7}^d$, take about 80 ms to settle to the new amplitudes because of the inserted low pass filters in Figure 3.17. Although these filters slow down the amplitude measurement performance, they are necessary for reducing the undesired effect of transient fluctuations of measured amplitudes on the adaptation to amplitude algorithm, as discussed in Section 3.7.1.

![Figure 3.26 Responses to a voltage sag at 300 ms, (a) measured phases and (b) measured amplitudes](image)

3.8.6 Case 6: FLL Performance

For the last case, the performance of the proposed FLL structure in Figure 3.16 is surveyed in Figure 3.27.
PI controller for integrated PLL was tuned based on the results in Table 3.3 with the damping factor of $k = 1$ for SOGI-QSG. The FLL gain parameter, $\gamma$, was chosen so
that a desired performance is achieved. A trade-off between the overshoot and settling time is considered and the value is chosen to be $\gamma = 29000$. The results show the response, $\phi_o$, $\omega_o$ and $N_f + \alpha$, to a $10^\circ$ small-signal step phase change followed by a 2 Hz step frequency change in the input signal, $\Delta \phi_i$ and $\Delta \omega_i$. The effectiveness of the proposed structure in rejection of the harmonic content of the input signal is observed in the steady-state responses.

In order to survey the harmonic measurement performance using the proposed FLL in the harmonic measurement structure in Figure 3.17 in place of the SRF-PLL, the response to a small phase change followed by a 2 Hz frequency change is simulated. A short step delay of 0.56 ms is entered into the input signal. Figure 3.28 shows that the harmonic stages have been able to follow the phase variations at the output, $\phi_{1,3,5,7}$, and adapt to the frequency variations with no steady state error.

![Figure 3.28 FLL measured phases in response to a short delay in the input signal at 300 ms followed by a 2 Hz frequency changes at 400 ms](image)

In order to observe the effectiveness of the proposed FLL structure as well as the adaptive averaging window, the response of the conventional FLL in Figure 3.14 to a 10$^\circ$ step phase change followed by a 2 Hz frequency change with a fixed window length is plotted in Figure 3.29. It can be observed that harmonic ripples have adversely affected the steady-state measurements. In addition to this, there is a high steady state error in the output phase and frequency, $\phi_o$ and $\omega_o$. The error is caused by the presence of harmonics in the input signal as obtained in (3.55).
Figure 3.29 (a) measured phase and (b) measured frequency by the conventional FLL and with a fixed window length in response to a phase change followed by a frequency change

3.9 EXPERIMENTAL STUDIES

The proposed algorithm was implemented and evaluated by using Hardware-in-the-Loop (HIL) testing with Typhoon HIL400 device. An introductory description for the operation of this device and its DSP interfacing is provided in Appendix A. This device generates a distorted AC signal so that its angle and frequency is measured by the algorithm. These measured values are fed back to the Typhoon in order to be displayed on the oscilloscope and captured. The HIL configuration is illustrated in Figure 3.30. The distorted signal made by typhoon, $v_i$, is sent to an analogue output (AO) pin so that it can be acquired by the ADC module of the DSP microcontroller. The calculated phase, $\theta_o$, frequency, $\omega_o$, and window length, $N$, can be made available on the digital output (DO) pins of DSP to be monitored by digital input (DI) pins of Typhoon. A ladder type DAC as illustrated in Figure 3.31 is
modelled and programmed in Typhoon to convert the monitored digital values to analogue values suitable for monitoring and displaying on the oscilloscope. In order to be able to display up to four parameters at the same time with only one DAC, the model is extended with a 4-channel selector to switch between four different digital input values repeated with a high rate. The emulated capacitor at each output holds the obtained analogue value when the corresponding channel is not selected.

Figure 3.30 (a) HIL test configuration for PLL algorithm implementation, and (b) experimental setup
The PLL algorithm is written in C language and compiled for TI TMS320F28335 DSP microcontroller which is a 32-bit floating point DSP Microcontroller. The 150 MHz clock speed and 6.25 MSPS ADC of this Microcontroller makes it fast enough for power electronic applications. The optimised compiled code takes about 15 $\mu$s to calculate the frequency and harmonic phases of the input signal which is about 45% of the sampling interval.

![Diagram of ladder type DAC model](image)

Figure 3.31 Ladder type DAC model in Typhoon HIL schematic editor with 4-channel selector

In order to realise a MAF, an array in memory is defined in order to store the MAF input values for the interval of the window length. A circular array is implemented with a moving pointer to store the sample values in a circular manner as illustrated in Figure 3.32. The pointer, $i$, has the address of the current input sample, $k$, and is decreased by one in every sampling step. Therefore, the next input values are stored in the previous pointer addresses one by one. The other pointer has the address of the oldest input sample in the window, $k-N_f$. If any of the pointers exceed the address of the first element of the array, they will jump back to the address of the last element in a circular manner. As already mentioned in Section 3.4, size of the array must be equal to the maximum length of the averaging window plus one, $N_f^{\text{max}}+1$, in order not to overwrite the array elements.
Because of the limited accuracy of the floating point values, repetitive floating point additions and subtractions in the MAF as well as in the integrator can lead to accumulation of round-off errors in the accumulator. When a small value is added to the accumulator which may already contain a large value, the low-order decimal digits of the small number may be lost because the result is rounded by the limited accuracy of the implemented floating point in the digital controller. Compensated summation algorithm [109] is used to compensate for the accumulation of error. The amount of introduced error in every addition cycle is calculated and reduced from the accumulator in the next cycle. Figure 3.33 shows the realisation of the compensated summation algorithm for a simple accumulator. The same approach is used for the accumulators of MAF and integrator.

Figure 3.33 Realisation of compensated summation algorithm

3.9.1 Case 1: Steady-State Performance

For the first case of study, steady-state measured voltage angles for the harmonics, $\theta_{0,3,5,7}$, is acquired as plotted in Figure 3.34 with the proposed PLL algorithm in Figure 3.17. The input signal, $v_i$, is the same as the signal for the simulation case. It is observed that angles and phases are measured as expected. The value of the voltage phase can be obtained by considering the origin of the plot as zero angle.
Figure 3.34 Steady-state measured angles of harmonic voltages of the input signal in orange (0.5 V/div), (a) first and third harmonics and (b) fifth and seventh harmonics (60°/div) in blue and green, respectively

3.9.2 Case 2: Small-Signal Performance

For the second case of study, small-signal step response of the SRF-PLL in Figure 3.2 to a 10° phase change is plotted in Figure 3.35 and Figure 3.36.
The measured phase, $\phi_o$, and the variation of measured frequency, $\omega_o$, as well as the window length, $N_f + \alpha$, are plotted. The results are consistent with the simulation results in Figure 3.19. The small steady-state ripples observed in the results are introduced by the DC offset of the input signal. The DC offset generates first order
harmonic ripples in the obtained $v_q$. However, the MAF designed for eliminating even order harmonics cannot eliminate the odd order harmonic ripples. They can be eliminated by measuring and removing the DC offset from the input signal. Nonetheless, with small DC offset, the amount of ripple is negligible.

![Figure 3.36 Window length (2 samples/div) in response to a 10° step phase change](image)

### 3.9.3 Case 3: Frequency Measurement Performance

This case as plotted in Figure 3.37 is the response to a step 2 Hz frequency change in the input signal. The results are consistent with the simulation ones in Figure 3.19. The frequency output, $\omega_0$, has followed the frequency variation of the input signal with no steady-state error, and the window length has been adjusted for the new measured frequency.
Figure 3.37 Response to a 2 Hz step frequency change, (a) measured frequency (6.67 Hz/div) and (b) window length (3 samples/div)

3.9.4 Case 4: Large-Signal Performance

For the fourth case, the response to a large-signal 100° step phase change is obtained. The results are illustrated in Figure 3.38 and Figure 3.39. Despite the large transient variations in the measured frequency, $\omega_o$, and window length, $N_f+\alpha$, the PLL has
settled to the new phase. The results are also similar to the simulation case in Figure 3.23. As mentioned in the simulation case, large transients in the measured frequency are limited by the frequency limiter in Figure 3.2 which is necessity for digital realisation of MAF, as discussed in Section 3.1 and 3.4.

Figure 3.38 Response to a 100° step phase change, (a) measured phase (40°/div), and (b) measured frequency (2 Hz/div)
Figure 3.39 Window length (7 samples/div) in response to a 100° step phase change

3.9.5 Case 5: Harmonic Measurement Performance

The response for this case of study is plotted in Figure 3.40.

Figure 3.40 Response to a small delay in the input signal, first, third, fifth and seventh harmonic phases (35°/div) in blue, red, green and orange, respectively
This case illustrates the measured harmonic phases, $\phi_{1,3,5,7}$, in response to an input signal delay of 0.56 ms, similar to the simulation case in Figure 3.24. Therefore, the implemented PLL of Figure 3.17 can follow the harmonic phase variations as well as the fundamental one, as expected from the simulation results.

### 3.9.6 Case 6: Harmonic Amplitude Measurement Performance

For the last case, the transient in the measured harmonic amplitudes, $V_{1,3,5,7}$, in response to a large phase changes is obtained as shown in Figure 3.41. The results are similar to the simulation case in Figure 3.25 and show the small variation of the measured amplitudes during the large-signal transients which do not considerably affect the adaptation of the loop gain to the amplitude of the harmonics. The steady-state values also show an accurate amplitude measurement.

![Figure 3.41](image)

**Figure 3.41** Response to a large delay, (a) first and third harmonic normalised amplitudes and (b) fifth and seventh harmonic normalised amplitudes (0.33 V/div), in blue and green, respectively

### 3.10 CONCLUSIONS

The single-phase SRF-PLL was modelled, and both the phase and frequency variations were included in the modelling. The controller was tuned for having satisfactory time and frequency responses, and the validity of the obtained model was proved via simulation results. Designed PLL algorithm showed to be able to follow
the phase and frequency of the input signal in presence of high harmonic pollution. Additionally, feedforward and predictor compensators were compared for improving the performance of the designed PLL with MAF, and feedforward showed to be more effective in large-signal responses.

In addition, the averaging filter showed to be effective in removing the harmonic contents from the $dq$ components and providing ripple free measurement of the frequency and phase of the input signal. Furthermore, a window resizing algorithm for the averaging filter was proposed in order to make the MAF adaptive to frequency variations so that the same performance is achieved even if the frequency of the input signal varies. The proposed algorithm for adaptive averaging window resizing was able to follow the input frequency variations smoothly and with a desirable speed. Furthermore, the issue of inaccurate frequency measurement of FLL in presence of harmonics was also surveyed and an effective solution was proposed.

The idea of SRF-PLL was extended in order to be able to measure the angle and the amplitude of harmonic contents of the input signal. A method was proposed in which a limited number of stacked PLLs were used for selective harmonic measurement. Moreover, the stages were made adaptive to the amplitude of harmonic voltages so that the transient performance of the stages is maintained for different and varying harmonic amplitudes.

Both the simulation and experimental results showed the effectiveness and the feasibility of the algorithms with a reasonable computational effort by the digital controller in order to achieve a satisfactory frequency and phase measurement in all the PLL stages. The measured harmonic angles and amplitudes will be used as the reference values for the converter control and grid voltage quality improvement algorithms in the following chapters.
In this chapter, first, structure and protection of DVR are briefly surveyed. Then, control of a DVR converter and design of the converter output filter are discussed. The designed control algorithm for reference tracking of the DVR which is based on the Internal Model Principle (IMP) is comprehensively explained. The control algorithm is extended to include the reference tracking of selected harmonic voltages and disturbance harmonic rejection. The harmonic voltage angles measured by the designed PLL are used for making a reference voltage synchronised to grid harmonics. For design of controller, an improved pole placement technique is proposed in order to maximise the disturbance rejection while maintaining desired stability margins and transient response.

In addition, a model-based loop delay compensation algorithm is introduced which makes the control design independent of the loop delay introduced by digital controller. Furthermore, an adaptive method is proposed in order to improve the delay compensation algorithm and also improve the stability of the control system in presence of the plant parameter variations. Simulation and experimental results are provided to show the effectiveness of the proposed algorithms.

4.1 DVR STRUCTURE

DVR is a voltage source converter (VSC) which can be used for different applications in distribution networks. It is connected in series with the line to inject a controlled amount of voltage. Hence, This component can inject or absorb both active and reactive power to the grid depending on the application [110]. For series injection of voltage to the grid, the VSC can either be connected directly to the grid while having a float supply voltage potential or connected through galvanic isolation by a transformer [111] as describe in the following.

4.1.1 Transformer Connected Converter

A common structure for DVR is to use a transformer to transfer the VSC voltage to a series injected voltage. The transformer ratio can be selected so that
converter voltage falls into a standard industrial voltage range. This type of connection has the advantage of ensured Basic Insulation Level (BIL). Transformer can also be used as part of converter output filter. If it is placed at the converter side, it can shape the first stage of an LC or an LCL filter and if placed at the grid side, it can be used as the last stage of an LCL filter.

However, this configuration has the disadvantage of increases losses and nonlinear behaviour of transformer which may limit the bandwidth of system. Moreover, low frequency injection transformers are costly and bulky, and they are not off the shelf transforms, because their voltage rating is defined by the required injection voltage.

4.1.2 Directly Connected Converter

Direct series injection with transformer-less DVRs has been reported in [112-114]. This configuration has the advantage of improved performance because of removed nonlinearity and voltage drop as well as increased bandwidth. DVR setup also has a low volume and weight because of eliminated bulky component.

However, this type has some drawbacks including more complicated protection of power electronics components because of removed BIL. In addition, converter topology needs to be more complex and more components are expected to be used. Furthermore, a high level of isolation to ground is required [111].

4.2 DVR PROTECTION

Series devices have some protection issues and have been investigated in [111, 115-117]. The two important protection issues of DVR happen during short circuits and the loss of grid connection. They must be protected against these faults.

4.2.1 Short Circuit Protection

During a short circuit, a high fault current flows through the series connected device. This can affect the operation of DVR or damage the DVR devices. Two control methods can be considered as follows.

**Passive protection of DVR**

When the short circuit currents are too high for the converter devices, the protection method is to bypass the converter by a primary-side bypass breaker across the injection transformer so that the converter and other existing protection devices are protected from damage [118]. By using this method, the VSC can be rated for
relative low currents. The mechanical protection is slow but robust, easily controlled and not expensive. However, the breaker must be rated so much that it can be closed in all the possible fault conditions.

**Active protection of DVR**

If the VSC is rated for the short circuit currents, it can actively clear the fault and reduce or increase the short circuit currents. For active control, the rating of VSC has to be so much that it can conduct short circuit currents and still be able to inject voltage into the grid. If a zero voltage injection during fault is desired, a zero state is commanded to the inverter and the load current flows in the diodes and the IGBT switches. The full bridge converter has two zero state conditions in which either the lower IGBT switches or the upper ones are turned on. However, high current rating increases the cost of DVR implementation.

Protection issues are also surveyed in [118], and an integrated Protection plan with thyristors, varistors and mechanical bypass is proposed. In this scheme, instead of turning the converter off, an alternative path for the fault current is provided. Anti-parallel thyristors because of their fast response can be used as the alternative path before a more robust mechanical bypass is activated. Varistors which are voltage dependant resistors can limit the voltage spikes across the converter.

In addition, the filter transformer ratio can limit the voltage at the secondary. The saturation level of the transformer can also be used to limit the current transfer [111]. Therefore, the rating of protection devices can also be decreased, if they are placed at the secondary side of the transformer.

**4.2.2 Loss of Grid Connection**

If the supply of grid is disconnected, there is a risk of damaging the neighbouring equipment of DVR [119]. In this case, as illustrated in Figure 4.1, DVR tries to compensate the voltage drop for the downstream network. The current loop is closed through the upstream network, and therefore, a voltage reversal occurs on the upstream network. The network also acts as a voltage divider for the DVR voltage. Hence, the DVR must be able to detect the supply breaking and bypass itself from the network. Proposed methods in [119] include a communication link from the recloser to DVR to command a turn off before the operation of the recloser. Another approach is to sense the power flow direction in the upstream network by DVR.
Moreover, stopping the voltage injection when very low supply voltage is detected is also suggested. However, this may lead to a bypass in the cases in which the supply line is still intact.

![Diagram](image)

**Figure 4.1 Simplified schematic for grid connection loss**

### 4.3 LC FILTER DESIGN

The structure of a single-phase DVR converter is illustrated in Figure 4.2. It consists of a full bridge inverter and an LC filter. It is placed in series with the network. Removing the DVR from the network is possible via a breaker in parallel to the output. It shorts the output of the converter so that the device has no effect of the grid. The transformer also provides another level of protection by isolating the inverter from the grid. In addition, it lets the converter supply be isolated from the network ground.

![Diagram](image)

**Figure 4.2 Diagram of DVR converter and feedback control**

The inductance of the filter consists of the leakage inductance of the injection transformer ($L_l$). The leakage inductance of the transformer is mostly caused by the air leakage flux, and therefore, its dependency on the winding current is not as much as the inductance of iron cored inductors. Hence, the value of $L_l$ is less affected by saturation with high winding currents which enter the transformer from the grid. The leakage inductance helps limit the impact of the PWM voltage of the bridge. In order
to improve the output voltage quality, a filter capacitor, $C_f$, absorbs the current ripples of the transformer so that the current fed to the grid only has negligible switching harmonic content. The leakage inductance value defines the ripple current. Equation (4.1) shows how the value of ripple current for the full bridge configuration with bipolar modulation is calculated [120].

$$\Delta I_{\text{ripple}} = \frac{V_{dc} T_{sw}}{2 L_t} \left(1 - m_a \cos \left(\frac{2\pi}{T_0} t\right)\right)^2$$  \hspace{1cm} (4.1)

where $m_a$ is the modulation index, $T_0$ is the period of mains voltage, $T_{sw}$ is the switching period, and $V_{dc}$ is the supply voltage. The equation is obtained by the assumption that voltage of filter capacitor ($C_f$) is equal to (4.2).

$$v_{C_f}(t) = V_{dc} m_a \cos \left(\frac{2\pi}{T_0} t\right)$$  \hspace{1cm} (4.2)

The maximum ripple current is then calculated as follows.

$$\Delta I_{\text{ripple}}^{\text{max}} = \frac{V_{dc} T_{sw}}{2 L_t}$$  \hspace{1cm} (4.3)

This ripple current as well as the grid current cause losses in the winding resistance. Additionally, the capacitor must be able to handle the losses of the ripple current associated with its internal Equivalent Series Resistor (ESR). The RMS ripple current is calculated by the assumption of a triangular waveform pattern for the ripple and is given in (4.4).

$$I_{\text{ripple}}^{\text{RMS}} = \sqrt{\frac{2}{T} \int_0^{T/2} [I_{\text{ripple}}(t)]^2 \, dt}$$  \hspace{1cm} (4.4)

$$= \sqrt{\frac{2}{3T} \int_0^{T/2} (\Delta I_{\text{ripple}} / 2)^2 \, dt}$$

$$= \frac{V_{dc} T_{sw}}{4 L_t} \sqrt{\frac{1}{8} m_a^4 - m_a^2 + 1}$$

The value of capacitance defines the voltage ripple at the converter output. The assumption of triangular current ripple waveform yields equation (4.5) for capacitor ripple voltage.

$$\Delta V_{\text{ripple}} = \frac{V_{dc} T_{sw}}{16 L_t C_f} \left(1 - m_a \cos \left(\frac{2\pi}{T_0} t\right)\right)^2$$  \hspace{1cm} (4.5)
Smaller ripples are desired in order to improve the voltage quality for switching harmonics at the output. However, increasing the value of capacitance leads to a decrease in the resonant frequency of the LC filter which is approximated by (4.6).

\[ f_r = \frac{1}{2\pi\sqrt{L/L_C}} \]  

(4.6)

The resonant frequency must be higher than the frequency of the highest order harmonic to be compensated in order not to degrade the controller performance for harmonic compensation. In addition, the disturbance effect on the output voltage is reduced with a higher resonant frequency because of the lower output impedance of the filter for the frequencies below the resonance. Nonetheless, for effective active damping of the resonance, this frequency must be one third to one twentieth of the controller gain crossover frequency so that the feedback controller has enough loop gain for damping the resonance. Therefore, when effective active damping is desired, the resonant frequency cannot be pushed to a very high frequency.

The transformer is assumed with 50 V\textsubscript{RMS} and 100 A\textsubscript{RMS} rating and 0.06 pu leakage reactance, and consequently, the value of \( L_i \) is 96 \textmu H. With 15 kHz switching frequency and 100 V DC supply, it gives the maximum of 34.9 A for \( \Delta I_{\text{max}}^{\text{ripple}} \) and 7.7 A\textsubscript{RMS} for \( I_{\text{ripple}}^{\text{RMS}} \). This ripple current is limited to 25% of the maximum current of the converter. With 200 \textmu F value for \( C_f \), the maximum of \( \Delta V_{\text{ripple}} \) is 1.5 V which is about 2% of the maximum output voltage. The resonant frequency is therefore, 1.15 kHz which is much higher than the first few harmonics to be compensated. It is also much less than the Nyquist frequency which is equal to 15 kHz for 30 kHz sampling rate. Therefore, with proper design of the controller, it will have enough bandwidth to actively damp the resonance and reject the high order harmonics of the disturbance. These values are summarised in Table 4.1.

<table>
<thead>
<tr>
<th>Table 4.1 The parameter values for the designed plant</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Sr, I_r )</td>
</tr>
<tr>
<td>( L_i )</td>
</tr>
<tr>
<td>( C_f )</td>
</tr>
<tr>
<td>( n:1 )</td>
</tr>
<tr>
<td>( V_{dc} )</td>
</tr>
</tbody>
</table>
The envelope of the ripple current and voltage for half a mains cycle are also plotted in Figure 4.3. The maximum reactive power absorption by the filter capacitor is recommended to comply with the condition given in (4.7) to limit the decrease in the power factor at the rated power to less than 5% [121]. The maximum reactive power absorption by capacitor is 157 VA which is 3.14% of the converter VA rating.

$$Q_{C_f}^{\text{max}} = C_f \omega_0 \left( V_{\text{RMS}}^{\text{max}} \right)^2 < 0.05 \times Q_{\text{rated}}$$  \hspace{1cm} (4.7)

In high power applications, the switching frequency is generally low and below 2.5 kHz [122]. The low switching frequency increases the amount of current and voltage ripples, and therefore, higher inductance and capacitor values may be required. The other important design aspect is the filter resonant frequency that could be in the order of switching frequency. The filter is usually designed for a resonant frequency below half of the switching frequency and much higher than the main frequency. However, in high power applications, because of the low switching frequency, further reducing of the resonance frequency may not be practical causing switching harmonics to trigger the filter resonance. In addition, active damping may not be possible, and therefore, passive damping of filter resonance through placing series or parallel resistors is necessary.
4.3.1 High Voltage DVR Design

For design of the LC filter for an LV-DVR, the injection transformer is directly connected to the inverter, and the filter capacitor is placed at the grid side as already illustrated in Figure 4.2. The leakage inductance of the transformer can be controlled by the design to be within a desired range. However, for high voltage (HV) design, the injection transformer is placed at the grid side to step down the HV to LV at the inverter side. The leakage inductance of this transformer is the line filter inductance. In addition, for limiting the inverter switching current ripples, air inductors are used and placed at the inverter output. A capacitor bank is also placed in the middle to shape an LCL filter [111]. The additional line filter inductance reduces the switching harmonic injection to the grid. However, the line inductance series to the grid causes losses and voltage drop at main and harmonic frequencies.

If a large HV-DVR is inserted in medium voltage (MV) distribution system, it can cover a larger number of buses. Nonetheless, a part of DVR capacity may be utilised for loads that do not require the provided voltage compensation by DVR. The introduced series impedance of the inserted DVR seen by LV network is relatively small compared to the line impedance, which is an advantage of using DVR in MV networks. The protection cost per MVA is also expected to be lower than that of multiple LV-DVR units [111]. However, a higher isolation level for DVR and injection transformer is required, because the short circuit current level is high.

Placing the DVR in LV distribution system has the benefit of lower short circuit level and easier protection. There is also flexibility in DVR placement across the LV network. However, the introduced series impedance is high and a proper converter control algorithm is required to actively reduce this impedance such that the voltage distortion caused by harmonic currents is reduced or eliminated. This impedance can also affect the short circuit level and protection.

DVR has higher efficiency and effectiveness in voltage compensation and quality improvement compared to D-STATCOM, and thus, DVR is an interesting device for power quality improvement. In this thesis, the better effectiveness of DVR compared to D-STATCOM is verified by simulations.
4.4 MODELLING OF THE CONVERTER

The continuous-time state space model of the plant consisting of the LC filter and the inverter can be obtained by considering the transformer current and capacitor voltage as two states. The grid current, $i_d$, which is generated by grid demand and generation is modelled as a current source disturbances as illustrated in Figure 4.4.

Figure 4.4 Small-signal model of the converter

The resistive loads on the grid can help in passive damping of the LC filter resonance. The resistive loads act as an equivalent parallel resistance for the filter and decrease the resonance strength. In addition, the equivalent inductance value of the reactive loads is much higher than the filter inductance value, and therefore, they do not have any considerable effect on the resonant frequency of the filter. The continuous-time state space model of the plant is obtained as given in (4.8).

\[
\begin{align*}
\dot{x} &= Ax + Bu + Ei_d \\
y &= Cx
\end{align*}
\]

\[
x = \begin{bmatrix} i_{L_f} \\ v_{C_f} \end{bmatrix}, \quad A = \begin{bmatrix} -\frac{r_w}{L_i} & -\frac{2r_{sw}}{n^2L_i} & -\frac{1}{L_i} \\ -\frac{1}{C_f} & 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} \frac{V_{dc}}{nL_i} \\ 0 \end{bmatrix}, \quad E = \begin{bmatrix} 0 \\ -\frac{1}{C_f} \end{bmatrix}, \quad C = \begin{bmatrix} 0 & 1 \end{bmatrix},
\]

(4.8)

where $L_i$ and $r_w$ are the transformer leakage inductance and wire resistance from the primary side (grid side), $r_{sw}$ is the on resistance of inverter switches, $n$ is the secondary to primary turn ratio of the transformer, and $v_{C_f}$ is the output voltage.

For digital realisation of a control system for a continuous-time plant, the controller can be designed in the continuous-time domain and then be discretised using Tustin, backward or forward Euler method [104]. This discretised control system is an approximation of the continuous-time one. On the other hand, it is possible to design the control system directly in the discrete-time domain. The discretised plant model must, therefore, be used for the design. The input voltage to the LC filter is a Pulse Width Modulated (PWM) signal with an average voltage equal to $u[k]V_{dc}$. For the
sampled current and voltages at the $k$-th sampling point, the effect of PWM voltage on the LC filter is equivalent to its average over the sampling interval. Therefore, the discretised PWM can be considered as a Zero Order Hold (ZOH) which samples the value of $u$ at each sampling point and holds it for the whole sampling interval. The plant with the assumption of a ZOH input is discretised as follows [104].

$$
A^z = e^{AT_s} = I + \sum_{i=1}^{\infty} \left( e^{AT_s} \right)^i, \quad B^z = A^{-1} \left( e^{AT_s} - I \right) B = T_s \left[ I + \sum_{i=1}^{\infty} \left( e^{AT_s} \right)^i \right] B, \quad E^z = A^{-1} \left( e^{AT_s} - I \right) E,
$$

(4.9)

where $T_s$ is the sampling interval, and $A^z$, $B^z$ and $E^z$ are the discretised state space matrices. Nonetheless, the disturbance current, $i_d$, has a sinusoidal continuous-time pattern, and its value between samples cannot be considered constant as ZOH assumption. Therefore, in order to find a more accurate discrete-time representation for $E$, the response of the plant to a sinusoidal disturbance during one sampling interval is considered. The overall solution for the state space equation with disturbance input can be written as given in (4.10) [123].

$$
x(t) = e^{A(t-t_0)} x(t_0) + \int_{t_0}^{t} e^{A(t-\lambda)} E I_d \cos(\omega_0 \lambda + \phi) d \lambda
$$

(4.10)

For considering the response during one sampling interval, $t_0$ is replaced with $kT_s$, and $t$ is replaced with $(k+1)T_s$. Furthermore, by a variable change as $\eta = (k+1)T_s - \lambda$, it yields,

$$
x\left[ (k+1)T_s \right] = e^{AT_s} x\left[ kT_s \right] + \int_0^{T_s} e^{A\eta} E I_d \cos\left[ \omega_0 (kT_s + T_s - \eta) + \phi \right] d \eta.
$$

(4.11)

Finding the solution gives (4.12).

$$
x\left[ (k+1)T_s \right] = A^{-1} \left( e^{AT_s} - I \right) x\left[ kT_s \right] + \left( I + A^{-2} \omega_0^2 \right)^{-1}
\times \begin{pmatrix}
A^{-1} \left( e^{AT_s} \cos(\omega_0 kT_s + \phi) - \cos(\omega_0 (k+1)T_s + \phi) I \right) \\
-\omega_0 A^{-2} \left( e^{AT_s} \sin(\omega_0 kT_s + \phi) - \sin(\omega_0 (k+1)T_s + \phi) I \right)
\end{pmatrix} E I_d
$$

(4.12)
This equation needs the derivative of the sinusoidal disturbance which is, in fact, the 90° phase shifted value of the disturbance, \( i^d_{\beta}[k] \), multiplied by \( \omega_0 \). It also needs the predicted disturbance value at the next sampling step \((k+1)\). The problem of this discretised model is that it needs the \( \alpha', \beta' \) components. In the single-phase, these components are made by using a phase shift filter, such as SOGI, which introduces some conversion delay. In order to avoid this, if the sampling intervals are very short, the sinusoidal disturbance during each sampling interval can be approximated by a First Order Hold (FOH) which is the linear approximation of the signal. The discretised input disturbance matrix is then obtained in (4.13).

\[
E_0^d i_{d,k} + E_1^d i_{d,k+1} = A^{-1} \left[ e^{A T_s} - A^{-1} \left( e^{A T_s} - I \right) T_s^{-1} \right] E i_{d,k} \\
+ A^{-1} \left[ A^{-1} \left( e^{A T_s} - I \right) T_s^{-1} - I \right] E i_{d,k+1},
\]

(4.13)

which is equivalent to the ZOH discretisation when \( i_{d,k+1} = i_{d,k} \). The equivalent discrete-time state space model of the plant is then given by (4.14).

\[
x_{k+1} = A^z x_k + B^z u_k + E_0^z i_{d,k} + E_1^z i_{d,k+1}
\]

(4.14)

Then, the plant transfer functions are calculated as given in (4.15).

\[
V_{C_f}(z) = C \left( zI - A^z \right)^{-1} B^z U(z) + C \left( zI - A^z \right)^{-1} \left[ E_0^z + E_1^z z \right] I_d(z)
\]

(4.15)

The future value of disturbance current at the next sampling point in a steady state, when it includes the fundamental component as well as its harmonics and with the assumption of a constant amplitude during the prediction period, can be predicted by considering the steady-state impulse response of addition of discrete-time resonant transfer functions for the harmonic frequencies, as derived in (4.16).

\[
I_d(z) = \sum_{h=1,3,\ldots} V_{1,n} z + V_{0,n} \frac{z^2 - 2 \cos(h \omega_0 T_s) z + 1}{z^2 - 2 \cos(h \omega_0 T_s) z + 1} \Delta(z)
\]

\[
\Rightarrow I_d(z) \times \prod_{h=1,3,\ldots} \left( z^2 - 2 \cos(h \omega_0 T_s) z + 1 \right) = 0
\]

\[
\Rightarrow z I_d(z) = z I_d(z) - z^{-h_{\text{max}}} \prod_{h=1,3,\ldots} \left( z^2 - 2 \cos(h \omega_0 T_s) z + 1 \right) I_d(z)
\]

\[
T_s \approx (h_{\text{max}} \omega_0)^{-1} \approx \left[ z - z^{-h_{\text{max}}} (z - 1)^{h_{\text{max}}+1} \right] I_d(z),
\]
where \( h \) is the harmonic order, and \( h_{\text{max}} \) is the maximum order of harmonic component present in the signal. Only odd harmonics are considered, because the amplitude of even harmonics in the grid current is negligible. This predicted value can be placed in (4.14) when the harmonic content is so high that it affects the accuracy of the disturbance prediction. Nonetheless, this equation is not valid during transients, and because of its derivative operation, can give large transient prediction errors. Therefore, it was used only for the prediction of the first few harmonics which have larger amplitudes than the higher order harmonics. Here, the discrete-time realisation of the prediction with the assumption of considerable amplitude for only the 1st and 3rd harmonics is obtained in (4.17).

\[
i_{d,k} + i_{g,k} = 4i_{d,k} - 6i_{d,k-1} + 4i_{d,k-2} - i_{d,k-3}.
\] (4.17)

### 4.5 MODELLING AND DESIGN OF THE CONTROLLER

According to Table 4.1, sampling rate is twice the switching frequency. This means that signals are sampled two times in every switching period, and PWM output is updated with the same rate. The control system is, therefore, discretised with this sampling rate. The higher sampling rate achieved by this method increases the gain crossover frequency of the controller which improves the active damping of the filter resonance and the disturbance rejection. The sampling and PWM patterns are depicted in Figure 4.5. \( D[k] \), in the figure, indicates the duty cycle which for the bipolar modulation is given in (4.18). It needs mentioning that digital controller is able to linearly set the value of duty cycle from 0 to 100 \% which means that the maximum linear modulation index, \( m_a \), is equal to 1.

\[
D[k] = \frac{1 + u[k]}{2}
\] (4.18)

Figure 4.5 shows that current ripples are filtered by the sampling pattern. However, capacitor voltage ripples are sampled, and they enter the control loop. They generate switching frequency ripples which are added to the control effort, \( u \). Since these voltage ripples are small and high frequency, they are finally averaged by the LC filter, and their effect on the control system performance, in both the current and voltage control, is negligible.
Having defined the sampling and PWM pattern, a control algorithm is required such that converter output voltage tracks the reference voltage with ideally zero steady-state error. The reference voltage for capacitor voltage is given in (4.19).

\[ v_{CF}^{ref}[k] = V_{DVR} \cos(\theta_{k}^{s1} + \phi_{DVR}) \]  

(4.19)

where \( V_{DVR} \angle \phi_{DVR} \) is the reference output phasor voltage, and \( \theta_{k}^{s1} \) is the reference angle obtained by a PLL from the grid voltage, \( V_{s1} \), in order to synchronise the converter with the grid voltage. Since the reference input of the control system is a sinusoidal signal, zero steady-state error is ideally realised by introducing an internal model of the reference input to the control loop. This idea for controller design is based on the Internal Model Principle (IMP) in which the compensator includes an internal model of the reference input [41]. Therefore, in this case, the compensator must be a resonant one which models the sinusoidal reference input.

The block diagram of the control system is displayed in Figure 4.6. It consists of the state feedback gains (\( K^c \)), the internal resonant model \( R(z) \) and the disturbance feedforward (\( F \)).

The internal resonant compensator adds two states to the control system. The compensator can be included in the state space model to obtain a state space model
for the whole system which simplifies the control design procedure. For this purpose, the compensator has been modelled by two resonant complex conjugate poles with complex conjugate feedback gains as given in (4.20).

$$R(z) = \frac{k_r/2}{z - e^{-(\omega_0 - j\omega_b)T_s}} + \frac{k_r/2}{z - e^{-(\omega_0 + j\omega_b)T_s}} = \frac{\text{Re}(k_r)z - e^{-\omega_0 T_s} \left[ \text{Re}(k_r)\cos(\omega_0 T_s) + \text{Im}(k_r)\sin(\omega_0 T_s) \right]}{z^2 - 2e^{-\omega_0 T_s} \cos(\omega_0 T_s)z + e^{-2\omega_0 T_s}}$$

(4.20)

where \(\omega_0\) is the main voltage frequency, and \(\omega_c\) is the cut-off frequency of the resonant compensator. The obtained transfer function in (4.20) is consistent with the transfer function proposed in [124, 125] given in (4.21) with \(\omega_c\) equal to zero.

$$R(z) = \frac{k_1z + k_2}{z^2 - 2\cos(\omega_0 T_s)z + 1}$$

(4.21)

However, the complex method is beneficial, if the resonant compensator is made adaptive to frequency variations by changing the value of the resonant frequency, \(\omega_0\). The frequency response of the compensator is less sensitive to the frequency adaptation compared to the other method. It is because both the zero with the value in (4.22) and poles are adjusted for the new resonant frequency such that the frequency response is only shifted, and its gain and phase are less affected.

$$z_1 = e^{-\omega_0 T_s} \left[ \cos(\omega_0 T_s) + \frac{\text{Im}(k_r)}{\text{Re}(k_r)} \sin(\omega_0 T_s) \right]$$

(4.22)

For including the new states in the model, the discrete-time block diagram of \(R(z)\) in the state space form, obtained from (4.20), is depicted in Figure 4.7.
The new states are called \( r_c \) and \( \overline{r}_c \), with the state feedback gains of \( k_r \) and \( \overline{k}_r \). By assuming \( v_{\text{ref}}^\text{ref} = 0 \), \( e \) equals to \(-y\), and equation (4.23) is obtained which is the z-domain equivalent of the state space equation for the new states.

\[
 z \begin{bmatrix} r_c \\ \overline{r}_c \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 0 \end{bmatrix} y + \begin{bmatrix} p_r & 0 \\ 0 & p_r \end{bmatrix} \begin{bmatrix} r_c \\ \overline{r}_c \end{bmatrix} = \frac{1}{2} C x^z \begin{bmatrix} 1 \\ 1 \end{bmatrix} + R \begin{bmatrix} r_c \\ \overline{r}_c \end{bmatrix}, \tag{4.23}
\]

where \( p_r = e^{-(\alpha t - \omega_0)j} \). Therefore, the state space model of the whole control system is obtained as given in (4.24).

\[
x^\text{IM} = \begin{bmatrix} i_{L_t} \\ v_{\text{cf}}^c \\ r_c \\ \overline{r}_c \end{bmatrix}, \quad A^\text{IM} = \begin{bmatrix} A^z & 0 \\ C/2 & R \end{bmatrix}, \quad B^\text{IM} = \begin{bmatrix} B^z \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad E^{\text{IM}0} = \begin{bmatrix} E^{z0} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad E^{\text{IM}1} = \begin{bmatrix} E^{z1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \tag{4.24}
\]

and with the state feedback coefficient matrix, \( K^{\text{IM}} \), as follows.

\[
 K^{\text{IM}} = \begin{bmatrix} K^z & k_r & \overline{k}_r \end{bmatrix} = \begin{bmatrix} k_{i_{L_t}} & k_{\text{cf}}^{\text{IM}} & k_r & \overline{k}_r \end{bmatrix}. \tag{4.25}
\]

For discrete-time realisation of the resonant compensator in DF-II, it must be considered that resonant filter is a high Q filter. In DF-II, the error input, \( e \), is first passed through an all-pole resonant filter which has two resonant poles. This all-pole filter works as an amplifier for the input signals in the range of the resonant frequency. Therefore, the value of the intermediate variable, \( w \), may overflow in a fixed point implementation, or it may become inaccurate in a floating point implementation because of the round-off error. Therefore, the transposed DF-II is used for discrete-time realisation, as illustrated in Figure 4.8.

The transposed DF-II realisation is also provided in (4.26).

\[
 r_k = v_{k-1}, \quad w_k = b_2 e_k - a_2 r_k, \quad v_k = w_{k-1} + b_1 e_k - a_1 r_k, \tag{4.26}
\]

where \( e \) is the tracking error and,
\[ b_1 = \text{Re}(k_r), \]
\[ b_2 = -e^{-\alpha T_s} \left[ \text{Re}(k_r) \cos(\omega_0 T_s) + \text{Im}(k_r) \sin(\omega_0 T_s) \right], \]
\[ a_1 = -2e^{-\alpha T_s} \cos(\omega_0 T_s), \]
\[ a_2 = e^{-2\alpha T_s}, \]

and,

\[
\begin{bmatrix}
\text{Re}(k_r) \\
\text{Im}(k_r)
\end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ -j & j \end{bmatrix} \begin{bmatrix} k_r \end{bmatrix}. \tag{4.28}
\]

Figure 4.8 Transposed DF-II realisation of the resonant compensator

### 4.5.1 Active Damping of Resonance

In (4.29), the transfer function of the plant with an added series resistor to the capacitor, \( r_s \), is shown. This resistor can act as passive damper for the filter resonance, because it increases the damping ratio of the second order system.

\[
G_{v_{\text{ CJ}/r}}^{\text{inner}} = \frac{V_{dc}/n}{L_i C_f s^2 + (r_s + r_{Ll}) C_f s + 1} \tag{4.29}
\]

In addition, (4.30) shows the closed loop transfer function of the inner loop in continuous-time domain consisting of the current and voltage state feedbacks.

\[
G_{v_{\text{ CJ}/r}}^{\text{inner}} = \frac{V_{dc}/n}{L_i C_f s^2 + \left(k_{i_{Ll}} V_{dc}/n + r_{Ll}\right) C_f s + 1 + k_{v_{\text{ CJ}}} V_{dc}/n} \tag{4.30}
\]

Comparison of the two transfer functions reveals that ideally current feedback works as a virtual impedance equal to \( k_{i_{Ll}} V_{dc}/n \) and is able to replace the effect of the series resistor, \( r_s \), for having a similar damping ratio by adjusting its feedback gain, \( k_{i_{Ll}} \). Nonetheless, the delay which exists in the discrete-time feedback loop reduces
the effectiveness of the active damping. The value of damping factor and resonant frequency is obtained in (4.31) which shows the effect of voltage feedback in shifting the resonant frequency to a higher frequency. This means that the output is less affected by high order disturbance harmonics and high frequency noise, because they get weaker as their frequency increases.

\[ \omega_n = \sqrt{\frac{1 + k_{cf} V_{dc}/n}{L_i C_f}}, \]

\[ \xi = \frac{r_{lf} V_{dc}/n}{2\sqrt{1 + k_{cf} V_{dc}/n}} \cdot \sqrt{\frac{C_f}{L_l}} \quad (4.31) \]

### 4.5.2 Controller Design for Selective Harmonic Tracking

If it is required from the converter to track a reference voltage which includes selected harmonic voltages as shown in (4.32), the control loop must have a high gain at the selected harmonic frequencies.

\[ v_k^{C_{ref}} = \sum_{h=1,3}^{\text{harmonic}} V_{DVR,h} \cos \left( \theta_{k,h}^{si} + \phi_{V_{DVR,h}} \right), \quad (4.32) \]

where \( h \) is the harmonic order, and \( \theta_{k,h}^{si} \) is the reference angle for each harmonic. In order to achieve this goal, resonant compensators \((R_h)\) can be stacked as shown in Figure 4.9 so that the error signal is fed through a high gain controller at all the selected harmonic frequencies. This minimises the tracking error at those frequencies. If a zero reference at a selected harmonic frequency is commended to the controller, the control system works as a notch filter for that disturbance harmonic, and the effect of that harmonic content on the converter output voltage is attenuated. These harmonics in the output voltage are the result of the limited output admittance of the converter when no compensation is incorporated.

![Figure 4.9 Implementation of stacked resonant compensators for harmonic tracking](image-url)
Each compensator is tuned in a selected harmonic frequency which is supposed to be tracked. Because of the small bandwidth of each stage, the paralleled compensators do not affect each other’s performance, and they are only able to react to the frequency content which is in the vicinity of their resonant frequencies. For the purpose of modelling, the state space model must include the new states for the extra stages. The same approach as the previous section is used for all the harmonic resonant compensators. The resultant state space model is given in (4.33).

\[
A^{BM} = \begin{bmatrix} A^z & C/2 & R_1 & 0 \\ C/2 & R_3 & \vdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ C/2 & R_{h_{\text{max}}} \end{bmatrix}, \quad B^{BM} = \begin{bmatrix} B^z \\ \vdots \end{bmatrix},
\]

(4.33)

\[
E_0^{BM} = \begin{bmatrix} E_0^z \\ 0 \\ \vdots \end{bmatrix}, \quad E_i^{BM} = \begin{bmatrix} E_i^z \\ 0 \\ \vdots \end{bmatrix}, \quad C^{BM} = [C \ 0 \ \cdots],
\]

in which,

\[
R_h = \begin{bmatrix} p_{r,h} & 0 \\ 0 & p_{r,h} \end{bmatrix},
\]

(4.34)

and \( p_{r,h} = e^{-(\omega_h - j\omega_0)T_s} \) is the resonant pole for each selected harmonic. The state feedback coefficient matrix, \( K^{BM} \), is, therefore,

\[
K^{BM} = \begin{bmatrix} K^z & k_{r,1} & k_{r,3} & \cdots \\ k_{r,1} & k_{r,3} & \cdots & \vdots \\ \vdots & \vdots & \ddots & \end{bmatrix} = \begin{bmatrix} k_{i_{LF}} & k_{v_{CF}} & k_{r,1} & k_{r,3} & \cdots \\ k_{i_{LF}} & k_{v_{CF}} & k_{r,1} & k_{r,3} & \cdots \end{bmatrix}.
\]

(4.35)

**4.5.3 Feedforward for Disturbance Rejection**

Feedback controller has high loop gain only at the limited selected resonant frequencies. But, in a steady state, disturbance has frequency contents at the other harmonic frequencies as well as the selected compensated ones. This causes the series connected converter to have a limited output admittance at these frequencies which results in a steady state tracking error and introduces considerable voltage drops in response to the disturbance current at these harmonic frequencies. Although disturbance frequency content becomes weaker at higher frequencies, the output admittance is also decaying at frequencies closer to the filter resonant frequency. Moreover, during disturbance current transients some high frequency contents also
exist in the disturbance current. Therefore, the feedback controller does not have enough loop gain to respond to these transients fast enough, and high transient tracking errors may appear.

This problem can be fixed by addition of more resonant compensators for the higher order harmonics. Since the compensation of harmonic voltages at these frequencies is not planned, the reference voltages for these frequencies are kept zero and therefore the response to disturbance current harmonics are controlled to a minimum. More resonant compensators need more computations by the digital controller. Nevertheless, since no other computations are performed for calculation of the extra harmonic reference voltages, the increased amount of computations are limited to only computing the discrete-time functions for the added compensators.

Apart from this, active damping was shown to be effective in increasing the output admittance. However, it can be improved, if a disturbance feedforward compensator is used. Feedforward can totally eliminate or reduce the disturbance effect on the system output. It works by measuring the disturbance current and giving a compensation response by directly manipulating the control effort. The effectiveness of the feedforward has been presented in [126]. This compensation is high bandwidth and fast, because it does not go through the feedback loop and is directly commanded to the control effort. Therefore, by a proper design for disturbance feedforward, the adverse effects of disturbance harmonics on the converter output voltage are effectively attenuated or eliminated, and the extra resonant compensators are not required.

The closed loop response of the system to disturbance with feedforward can be obtained as given by (4.36). It shows that for more effective disturbance rejection, the predicted value of $i_d$ must be fed through the feedforward as well.

$$G_{cf}/i_d = C^{IM} \left( z I - A^{IM} + B^{IM} K^{IM} \right)^{-1} \left( E_0^{IM} + E_1^{IM} z + B^{IM} \left[ F_0 + F_1 z \right] \right) \quad (4.36)$$

The response magnitude must be minimised by defining appropriate values for feedforward coefficients, $F_0$ and $F_1$, so that the dependency of the output to disturbance is minimised. A simple method is to find these values based on the steady-state response so that feedforward eliminates the effect of disturbance on the steady-state response of the output. This is not an optimum solution, because it does not consider transients. However, because it could improve the disturbance rejection
for a wide frequency range, it is also effective during transients. The response to
disturbance in a steady state is given by (4.37).

\[ y(\infty) = \lim_{z \to 1}(z-1)Y(z) \]

\[ = \lim_{z \to 1}C^{IM} \left( zI - A^{IM} + B^{IM}K^{IM} \right)^{-1} \]

\[ \times \left( E_0^{IM} + E_i^{IM}z + B^{IM} \left[ F_0 + F_i z \right] \right) (z-1)I_d(z) \]  (4.37)

This term must be zero in a steady state. \( i_d \) includes the fundamental component as well as harmonics, and it may also contain a DC component. Some methods have been presented in which the feedforward takes the advantage of using resonant compensators in the feedforward loop for selective disturbance harmonic rejection [127]. However, by considering \( i_d \) as DC, a simpler implementation is achieved which is effective in the whole frequency range, especially at low frequency range in which most of the disturbance harmonics exist. By replacing \( I_d(z) \) with the \( z \)-transform of the step function and equating (4.37) with zero, the proportional feedforward terms are obtained as given in (4.38).

\[ F_0 = - \left( C^{IM} \left( zI - A^{IM} + B^{IM}K^{IM} \right)^{-1} B^{IM} \right)^{-1} C^{IM} \left( zI - A^{IM} + B^{IM}K^{IM} \right)^{-1} E_0^{IM}, \]

\[ F_1 = - \left( C^{IM} \left( zI - A^{IM} + B^{IM}K^{IM} \right)^{-1} B^{IM} \right)^{-1} C^{IM} \left( zI - A^{IM} + B^{IM}K^{IM} \right)^{-1} E_i^{IM}. \]  (4.38)

### 4.5.4 Calculation of the System Transfer Functions

The closed inner loop transfer function including only the current and voltage state feedback, the control system open loop transfer function, the closed loop transfer functions from the reference input and disturbance input to control effort and output are given in (4.39) to (4.45).

\[ G_{\text{inner - loop}}^{\text{open - loop}} = C \left( zI - A^z \right)^{-1} B^z \]  (4.39)

\[ G_{\text{inner}}^{\text{v}_c f} = C \left( zI - A^z + B^zK^z \right)^{-1} B^z \]  (4.40)

\[ G_{\text{open - loop}} = K^{IM} \left( zI - A^{IM} \right)^{-1} B^{IM} \]  (4.41)

\[ G_{u/cf}^{\text{off}} = \left( 1 - K^{IM} \left[ zI - A^{IM} + B^{IM}K^{IM} \right]^{-1} B^{IM} \right) R(z) \]  (4.42)
\[ G_{v_{cf}} \big|_{\text{ref}} = C_{IM}^{-1} \left( zI - A_{IM} + B_{IM} K_{IM} \right) B_{IM} \left( z - \right) \] (4.43)

\[ G_{u_{id}} = -K_{IM}^{-1} \left( zI - A_{IM} + B_{IM} K_{IM} \right) \left( E_{0_{IM}} + E_{1_{IM}} z + B_{IM} \left[ F_{0} + F_{1} z \right] \right) \] (4.44)

\[ G_{v_{cf}} \big|_{\text{id}} = C_{IM}^{-1} \left( zI - A_{IM} + B_{IM} K_{IM} \right) \left( E_{0_{IM}} + E_{1_{IM}} z + B_{IM} \left[ F_{0} + F_{1} z \right] \right) \] (4.45)

where,

\[ R \left( z \right) = R_1(z) + R_3(z) + \cdots \] (4.46)

### 4.5.5 Pole Placement Technique

In order to find appropriate state feedback gains pole placement technique is used [42]. Poles must be placed such that the minimum stability margins as well as a desirable transient response are satisfied. At first, Linear Quadratic Regulator (LQR) method is used for finding an optimal placement. Because of the difficulty in achieving the desired margins by changing the weighting values, the results of this method is used and modified in order to achieve the desired control performance.

The harmonic compensators introduce additional poles to the loop transfer function. By using LQR method, they are placed on an arc close to the unity circle at the resonant frequencies of \( p_{r,h} \). In addition, the resonant compensators, \( R_h(z) \), introduce some zeros to the control loop which form the closed loop zeros of the system. These zeros are also located on an arc with smaller radius and still close to the unity circle and their corresponding resonant poles so that the phase lag caused by the resonant poles in the loop transfer function is compensated by nearby zeros. The zeros are placed with an angle at about half way between two adjacent resonant poles as given in (4.47). The number of these zeros is one less than the number of the resonant compensator poles as illustrated in Figure 4.10.

\[ z_{4,5,\ldots} \approx r_{4,5,\ldots} e^{\pm j(m\omega f_s)} \], \( m = 0, 2, 4, \ldots \) (4.47)

As the transfer function of resonant compensator in (4.20) shows, place of the zeros in the open loop transfer function is also dependent on the feedback gain and pole placement. Therefore, closed loop poles should not be placed far from their open loop locations. This makes them stay close to their corresponding resonant zeros so that their phase compensation effect is preserved. This makes the phase lag of the loop not affected considerably by the introduced stacked resonant compensators.
However, the closer the zero and poles are, the less resonant gain is achieved by the resonant compensator. Figure 4.10 shows the desired closed loop pole placement and the open loop pole-zero map plot in which closed loop poles are placed at half way angle between two adjacent resonant poles with a radius of $r_p = 0.985 \ [42]$. This radius is chosen so that the maximum calculated tracking errors at resonant frequencies is less than 0.5 %. With the same radius for the pole locations, a similar loop gain is also achieved for all the resonant stages. Therefore, poles are placed as given in (4.48).

$$p_{4.5,\cdots} = r_{p_{4.5,\cdots}} e^{\pm j(m\omega r_s)}, \ m = 0, 2, 4, \cdots \tag{4.48}$$

![Pole-zero map plot](image)

Figure 4.10 Pole-zero map plots of resonant compensators for the closed loop (red) and the open loop (blue) transfer functions, and the arrows indicating the movement of poles.

For effective active damping, the gain crossover frequency of the control loop must be three to twenty times higher than the filter resonant frequency so as to be able to compensate the resonance and attenuate the output response to disturbance. The plant has two resonant poles with the resonant frequency calculated in (4.49).

$$\omega_r = \frac{1}{\sqrt{L_f C_f}} = 7.236 \text{krad} / \text{s} \tag{4.49}$$
These poles are moved towards the $z = 0$ point to form the complex conjugate dominant poles. These poles and the last remaining pole will shape a third order system and determine the bandwidth and gain crossover frequency of the control system, stability margins, resonance damping and disturbance rejection. The bandwidth of the system must be sufficiently smaller than the Nyquist frequency, $\pi/T_s$. A limit of $0.5 \pi/T_s = 7500 \times 2\pi$ krad/s is recommended [104]. The dominant complex conjugate poles are placed as given in (4.50).

$$p_{1,2} = r_{p1,2} e^{\pm j \theta_s T_s} \quad (4.50)$$

The third pole, which is left from the resonant compensators, is also moved towards the $z = 0$ on the real axis as given in (4.51). It can be moved so much that its effect on the complex conjugate poles is minimised. However, this needs a high control effort and may lead to saturation of the control effort, and therefore, non-linearity in the control loop. This may cause the instability of the control loop.

$$p_3 = r_{p3} \quad (4.51)$$

For pole placement, maximising the bandwidth and gain crossover frequency is the target. This maximises the disturbance rejection and active damping. The limits are the stability margins and control effort. The limits of 45° phase margin and 8 dB gain margin are set for the open loop transfer function. The converter is linear up to $m_a$ equal to 1, and the rated voltage of the converter with a 100 $V_{dc}$ source voltage is 50 $V_{RMS}$ which is equal to 70.7 $V_p$. This means that a maximum of 41 % overshoot can be reached in the linear region of the converter for the rated output voltage. To have a margin due to the source and switch voltage drops and disturbance effects, the overshoot of control effort is limited to 20 % ($m_a = 0.85$) so as to avoid nonlinearities.

These three poles are placed by a configuration similar to the Butterworth Placement in continuous-time domain [128]. The matched placement in the discrete-time domain is given in (4.52).

$$p_{1,2} = r_{p1,2} e^{\pm j \theta_s T_s} = e^{-r_s T_s \cos \theta_s} \cdot e^{\pm j r_s T_s \sin \theta_s} \quad (4.52)$$

$$p_3 = r_{p3} = e^{-r_s T_s},$$

where $r_s$ is the matched radius of the placement in the continuous-time domain which defines the bandwidth. $\theta_s$ is the matched angle of placement of complex conjugate poles.
poles in the continuous-time domain. For the third other Butterworth filter, \( \theta_s \) is equal to 60°.

In order to find the proper values for \( r_s \) and \( \theta_s \), a software routine finds the value of stability margins while increasing the bandwidth by increasing \( r_s \) step by step and performing the placement in each step. The placement with the highest value of \( r_s \) in which the above mentioned limits for margins are not violated is considered as the desired pole placement. Using this method, the maximum bandwidth and disturbance rejection is achieved. The time domain response of the control effort is, then, simulated in order to find the overshoot. If the overshoot is higher than the defined limit, \( \theta_s \) is decreased, and the program is performed again until the overshoot limit is satisfied. Decreasing this parameter moves the poles closer to the real axis and increases the damping which reduces the overshoot.

### 4.5.6 Calculation of Feedback Coefficients

The state feedback coefficients for the desired pole placement in discrete-time domain are calculated by using the Ackermann’s formula, as given in (4.53).

\[
K^{BM} = [\begin{bmatrix} 0 & 0 & \cdots & 1 \end{bmatrix} \times \begin{bmatrix} B^{BM} & A^{BM} & B^{BM} & (A^{BM})^2 & B^{BM} & \cdots \end{bmatrix}]^{-1} \times P \left( A^{BM} \right), \quad (4.53)
\]

where \( P \) is the polynomial whose roots are the desired places for poles of the system. The problem of this equation is when the dimensions of the matrices are high, i.e. there are a number of resonant compensators in the control loop. As the number of resonant compensators is increased, and consequently, the dimensions of the matrices in the equation rise, the accuracy of the numerical calculations deteriorates due to round-off error. The \( \delta \) operator in (4.54) can improve the numerical accuracy of finite-word-length calculations including both the fixed point and floating point calculations [129].

\[
\delta = \frac{q - 1}{\Delta}, \quad (4.54)
\]

where \( q \) is the shift operator, and \( \Delta \) can be equal to the sampling interval or a free parameter to minimise the round-off error [130]. By assuming \( \Delta \) equal to one and by replacing (4.54) in the state space model of the system and solving for \( \delta x \), a modified state space model for the system is obtained, as given in (4.55), which improves the numerical accuracy of the matrix calculations.
\[ A_{\Delta}^{IM} = A^{IM} - I \]  

(4.55)

By replacing \( A_{\Delta}^{IM} \) in (4.53), more accurate feedback coefficients for a desired placement are calculated with even a high dimension of state space model matrices.

### 4.5.7 Control Design Results

Some parameters of the designed control system are summarised in Table 4.2. Five resonant compensators are stacked in order to be able to compensate the odd harmonics up to the 9th harmonics.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_c )</td>
<td>0.5 ( \times 2\pi ) rad/s</td>
</tr>
<tr>
<td>( r_{p1,2} )</td>
<td>0.752, ±0.214 rad</td>
</tr>
<tr>
<td>( r_{p3} )</td>
<td>0.7</td>
</tr>
<tr>
<td>( r_{p4,\ldots,12} )</td>
<td>0.985</td>
</tr>
</tbody>
</table>

The closed loop and open loop pole-zero map plots are depicted in Figure 4.11. It shows the movement of resonant poles of filter towards the \( z = 0 \).

![Pole-zero map plot](image-url)

Figure 4.11 Pole-zero map plots for the open loop (blue), and the closed loop (red) transfer functions
The closed loop frequency response of the inner loop in (4.40) as well as the open loop frequency response of this loop in (4.39) is plotted in Figure 4.12. As discussed in Section 4.5, the state feedback works as an active damper and attenuates the resonance of LC filter. The figure also shows the response in presence of one sampling interval loop delay as discussed in Section 4.6. The system with loop delay has poles outside the unity circle and has become unstable. This shows that loop delay can adversely affect the active damping to a great extent.

![Inner loop frequency response Bode Diagram](image)

Figure 4.12 open inner loop (blue), closed inner loop (red), and closed inner loop with delay (magenta) Bode plots

In order to show the control system performance, the open and closed loop frequency response Bode plots are illustrated in Figure 4.13. The resonant gain at the selected harmonic frequencies can be observed in the open loop bode plot. The closed loop gain and phase at the selected frequencies of 50, 150, 250, 350 and 450 Hz is controlled to about 0 dB.
Figure 4.13 (a) Open loop Bode plot, and (b) closed loop bode plot

In addition, in order to observe the disturbance rejection performance of the control system, Bode plots of response to disturbance transfer function of (4.36) with and
without the feedforward are illustrated in Figure 4.14. The frequency response is obtained with the assumption of the perfect prediction of disturbance. It can be observed that the proportional feedforward has been able to improve the disturbance rejection especially at lower frequencies. Also, the control system works as a notch filter at the selected harmonic frequencies and rejects these disturbance frequency contents more effectively.

Figure 4.14 Output closed loop response to disturbance without feedforward (blue), and with feedforward (red)

Table 4.3 shows the frequency response performance of the designed control system. Transient response analysis is also performed. In order to reduce the transient effects when DVR controller is enabled, its breaker is opened when the disturbance current crosses zero, i.e. \( I_d \cos(\theta_k) \) equals to zero, and consequently, \( \theta_k \) is ±90°. In addition, as discussed in Chapter 5, to minimise the active power consumption of DVR, the phase of filter capacitor voltage is 90° shifted from phase of disturbance current. Therefore, the voltage reference is \( V_{Cj} \cos(\theta_k + 90°)s[k] \) which shows that it has a step change at the start-up moment. This can be fixed by forcing a ramp limited reference voltage at start-up. However, the transient response performance to
this step reference, \( V_{c_f}^{\text{max}} \cos(\omega_b k T_s) s[k] \), is provided in Table 4.3 as the response to a worst case condition.

| Table 4.3 Frequency response and transient step response performance |
|-----------------|-----------------|-----------------|
| Min. disturbance rejection | without feedforward | -2.6 dB at 1.45 kHz |
|                      | with feedforward  | -13.5 dB at 2.22 kHz |
| Steady-state gain error at \( \omega_{in}, 3\omega_{in}, 5\omega_{in}, 7\omega_{in}, 9\omega_{in} \) | \(-38.6, -35.5, -28.4, -15.6, 9.88 \times 10^{-3} \) dB |
| Steady-state phase error at \( \omega_{in}, 3\omega_{in}, 5\omega_{in}, 7\omega_{in}, 9\omega_{in} \) | \(-25.6, -76.6, -126, -167, -167 \times 10^{-3} \)° |
| Phase margin, gain margin | 45°, 8.3 dB |
| Gain crossover frequency | 4 kHz |
| Maximum \( m_a \) | 0.85 |
| Output overshoot | 32% |
| Settling time | 10.3 ms |

### 4.6 LOOP DELAY COMPENSATION

Digital controllers need some time for their control computations. This time interval includes acquiring current and voltage samples, performing synchronisation, voltage reference and control effort calculation and updating the output PWM. This adds some delay to the control loop which increases the phase lag of the control loop transfer function, and therefore, reduces the phase margin. A delay equal to one sampling interval introduces a phase lag of \( 360 \times f_{\text{crossover}} \times T_s = 48° \) at the gain crossover frequency of the designed control system which reduces the phase margin by the same amount and can result in instability. Redesign of the controller with consideration of the delay may be helpful for stabilising the system, but it needs decreasing the bandwidth of controller in order to lower the gain crossover frequency. This reduces the effectiveness of active damping and disturbance rejection of the controller.

The digital controller has one sampling interval as the maximum period for the computations, and the PWM is updated at the next sampling point. Therefore, a fixed delay equal to one sampling interval exists for control effort update (\( z^{-1} U(z) \)). This means that one new state has entered the control loop. It also needs mentioning that PWM output which is averaged as ZOH with the transfer function in (4.56) introduces a delay approximately equal to half a sampling interval (a quarter of switching period).
Phase lag of the PWM delay can be compensated by using phase lead compensation. However, it adds new states to the control loop which must be included in the state feedback analysis of the control system. Therefore, the compensation of this intrinsic delay is overlooked, and since it is already included in the discrete-time plant model, with proper design of the controller enough stability margins can be achieved.

In order to compensate the computation delay, a predictor can be used to predict the values of the states at the next sampling point \( (x_{k+1}) \). The prediction pattern for one computation period is illustrated in Figure 4.15. The predicted control signal, \( u_p = u_{k+1|k} \), is calculated by using the predicted sample values. Thus, the control signal which will be applied at \( k+1 \) sampling point would have been made by using the predicted state values for \( k+1 \) sampling point.

![Sampling and prediction pattern](image)

The prediction can be performed independent of the plant model. Linear or slope based predictor predicts the future values of the states with the assumption of a linear pattern for the state values during the prediction period. The transfer function of this predictor for prediction of one sampling interval ahead is given in (4.57).

\[
P(z) = 2 - z^{-1}
\]  

(4.57)

It adds a second state to the system, and also, its predictions are not valid at high frequencies. A better method is to use a phase lead compensator to compensate the phase lag of the delay. It can be obtained by considering the few first terms of the Taylor series of \( e^{-sT_s} \) and discretising the transfer function by using Tustin
transform. The inverse of the discretised transfer function has a phase lead which can compensate the phase lag for a higher range of frequencies.

\[
\left( e^{-sT_s} \right)^{-1} \frac{\text{Tustin}}{z^2 + 2z + 1} = \frac{z^2 + 2z + 1}{z^2 - 2z + 5} \tag{4.58}
\]

This method has also the problem of added states as well as the limited frequency range. The new states as well as the delay state must be included in the state feedback analysis for determining the new state feedback gains.

An ideal approach is to use a model-based predictor which can theoretically compensate the delay for the whole frequency range and cancel out the introduced delay pole from the system. By using this predictor, the control design is simplified and the delay is not considered in the control design procedure. Although model inaccuracies do not let a perfect pole-zero cancellation, this approach is still effective in minimising the delay effect on the system, if inaccuracies are small. Adaptation of the model to plant parameter variations is helpful in reducing the prediction error as discussed in Section 4.7.

For realising a model-based predictor, the discrete-time state space model of the system in (4.9) and (4.13) can be used for prediction of the state values as calculated in (4.59).

\[
Z^{-1}\{zX(z)\} = x_{k+1|k} = \hat{x}_p^z
= \hat{A}^z x_k^z + \hat{B}^z u_{p-1} + \hat{E}_0^z i_{d,k} + \hat{E}_1^z i_{d,k+1|k},
\tag{4.59}
\]

where \( \hat{x}_p^z \) is the predicted state values at the next sampling point, \( \hat{A}^z, \hat{B}^z, \hat{E}_0^z \) and \( \hat{E}_1^z \) are the discrete-time prediction model state space matrices, and \( u_p \) is the predicted required control effort. \( u_p \) is calculated using (4.60) and (4.62).

\[
u_p = u_{k+1|k} = r_{p,1} + r_{p,2} + \cdots + \textbf{K}^z x_p^z + F_0 i_{d,k+1|k} + F_1 i_{d,k+2|k},
\tag{4.60}
\]

where \( r_p \) is the predicted output of resonant compensator. As observed in (4.62), the disturbance current, \( i_d \), needs to be predicted for up to two sampling intervals ahead by using the disturbance prediction equation of (4.17). With transformed DF-II realisation for resonant compensators, the predicted resonant terms in (4.60), \( r_{p,h} \) are calculated as given in (4.61).
\begin{align}
    r_{p,h} &= v_{p-1,h}, \\
    w_{p,h} &= b_{2,h}e_p - a_{2,h}r_{p,h}, \\
    v_{p,h} &= w_{p-1,h} + b_{1,h}e_p - a_{1,h}r_{p,h}, \\
    e_p &= \left(v_{p,ref}^C - v_{p}^C\right),
\end{align}

(4.61)

where $e_p$ is the predicted tracking error. In addition, as discussed in Chapter 3, $v_{s1}$ is sampled at the beginning of each sampling period, $k$, and the calculated $\theta_{k+1}$ by PLL is equal to the phase angle of voltage at the next sampling step ($p = k+1$), i.e. $\theta_p = \theta_{k+1}$. This value is, then, used for calculation of the reference voltage. Thus, the calculated reference voltage is, in fact, the predicted value of this voltage at the next sampling point as given in (4.63).

\begin{equation}
    v_{p,ref}^C(t) = \sum_{h=1,3,5,...} V_{DVR,h} \cos\left(\theta_p + \phi_{DVR,h}\right),
\end{equation}

(4.63)

where $\theta_{k,h}$ is reference angle for each harmonic which is obtained from $V_{s1}$ by PLL.

The block diagram of the internal model control system with predictor is depicted in Figure 4.16.

Figure 4.16 Block diagram of the control system with delay and predictor compensator

In order to have a perfect prediction, the prediction model matrices must contain the real parameter values from the plant. In this case, the delay pole is cancelled out by the predictor, and the transfer functions obtained in Section 4.5 are valid for analysis of the system performance. However, when modelling inaccuracies exist, control loop transfer functions can be obtained by finding the transfer function of the prediction functions. By considering the block diagram of Figure 4.16, the plant response is given in (4.64).

\begin{equation}
    X_p^{IM}(z) = \left(zI - A^{IM}\right)^{-1} \left[ B^{IM} z^{-1} U_p(z) + E_0^{IM} + E_1^{IM} z I_d(z) \right]
\end{equation}

(4.64)
Therefore, the response of the predictor is calculated in (4.65) and represented in terms of new defined matrices, $\mathbf{B}_p^{IM}$ and $\mathbf{E}_p^{IM}$.

$$
\mathbf{X}_p^{IM} (z) = \left[ \hat{A}^{IM} \left(zI - A^{IM}\right)^{-1} \mathbf{B}^{IM} + \hat{B}^{IM} \right] z^{-1} U_p (z) 
+ \left[ \hat{A}^{IM} \left(zI - A^{IM}\right)^{-1} \left( \mathbf{E}_0^{IM} + \mathbf{E}_1^{IM} z \right) + \left( \hat{E}_0^{IM} + \hat{E}_1^{IM} z \right) \right] I_d (z) \tag{4.65}
$$

$$
= \mathbf{B}_p^{IM} (z) U_p (z) + \mathbf{E}_p^{IM} (z) I_d (z) 
$$

The predicted control effort is then calculated as given in (4.66).

$$
U_p (z) = V_p^{C_{ref} (z)} R (z) - \mathbf{K}^{IM} \mathbf{X}_p^{IM} (z) + (F_0 + F_1 z) I_{d,p} (z), \tag{4.66}
$$

where index $p$ indicates the predicted value of samples, disturbance input and the reference input for $k+1$ sampling point. The transfer functions of the system with delay compensator are obtained in (4.67) to (4.71).

$$
G_{\text{open-loop}} = \mathbf{K}^{IM} \mathbf{B}_p^{IM} 
$$

$$
G_{u/I_c^{\text{ref}}} = \left( 1 + \mathbf{K}^{IM} \mathbf{B}_p^{IM} (z) \right)^{-1} R (z) \tag{4.68}
$$

$$
G_{y_c^{\text{ref}}} = \mathbf{C}^{IM} \left(zI - A^{IM}\right)^{-1} \mathbf{B}^{IM} \left( 1 + \mathbf{K}^{IM} \mathbf{B}_p^{IM} (z) \right)^{-1} R (z) \tag{4.69}
$$

$$
G_{u/I_d} = \left( 1 + \mathbf{K}^{IM} \mathbf{B}_p^{IM} (z) \right)^{-1} \left[ F_0 + F_1 z - \mathbf{K}^{IM} \mathbf{E}_p^{IM} (z) z^{-1} \right] \tag{4.70}
$$

$$
G_{y_c^{\text{ref}}} = \mathbf{C}^{IM} \left(zI - A^{IM}\right)^{-1} \left[ \left( \mathbf{B}^{IM} \left( 1 + \mathbf{K}^{IM} \mathbf{B}_p^{IM} (z) \right)^{-1} \right) \times \left( F_0 + F_1 z - \mathbf{K}^{IM} \mathbf{E}_p^{IM} (z) z^{-1} \right) \right] + \mathbf{E}_0^{IM} + \mathbf{E}_1^{IM} z \tag{4.71}
$$

With the condition of perfect prediction, these transfer functions are equal to the transfer functions in (4.41) to (4.45) calculated for the case with no delay. The advantage of this predictor compared to Smith predictor is that the recent samples as well as the control effort are used for prediction, while in the other method only control effort is used, and prediction is dependent on the previously calculated values of the states in the prediction model. Thus, this makes the method sensitive to plant parameter variations and error accumulation. Therefore, the predicted values by the proposed method are more accurate and less sensitive to parameter variations.
The accuracy of prediction defines the efficiency of delay compensation. Active damping, disturbance rejection and reference tracking are dependent on the accuracy of the prediction. More accurate prediction leads to having frequency response closer to the ideal case with no delay. For disturbance prediction, however, as mentioned in Section 4.4 the accuracy of prediction can only be guaranteed in a steady state and is also dependant on the number of harmonics included in the disturbance prediction equation. Therefore, the frequency response from disturbance to output with an accurate prediction and also ZOH approximation for future values of \( i_d \) are compared. In the latter case, the value of \( i_d \) is assumed to be constant during the prediction interval. In other words, the terms \( i_{d,k+1} \) and \( i_{d,k+2} \) in (4.59) and (4.60) are replaced with the current sampled value of the disturbance, \( i_{d,k} \), and the transfer functions are recalculated with this assumption. Figure 4.17 shows the bode plots for the two cases. They show that the ZOH prediction of disturbance causes to have about 5.4 dB attenuation in the disturbance rejection which is very low compared to the high rejection amount provided by feedforward.

![Frequency response to disturbance Bode diagram](image)

Figure 4.17 Output closed loop response to disturbance with (red) and without (blue) prediction of disturbance
4.7 ADAPTIVE PREDICTION MODEL

Because of measurement inaccuracies, tolerances and usage, some inaccuracies may enter the prediction model. Moreover, the DC bus voltage may also be variable, but it is easily measurable, and its variations can be included in the prediction model. In order to find the robustness of the system to model inaccuracies, a condition in which the real $C_f$ value is 25% less than the value in the prediction model and real $L_l$ value is 10% less than the model value is assumed. The results for the control system performance are summarised in Table 4.4. It shows that the stability of the system is preserved even with prediction model inaccuracies. However, compared to the results in Table 4.3, phase margin is reduced. The steady-state errors have not been affected considerably because of the small prediction interval. An online or offline method for estimation of plant parameters can be implemented to improve the control performance.

<table>
<thead>
<tr>
<th>$L_l$</th>
<th>-10%</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_f$</td>
<td>-25%</td>
</tr>
</tbody>
</table>

Table 4.4 Control performance with plant parameter variations

| Steady-state gain error at $\omega_0$, 3$\omega_0$, 5$\omega_0$, 7$\omega_0$, 9$\omega_0$ | -38.7, -35.7, -29.1, -16.7, 8.0 $\times 10^{-3}$ dB |
| Steady-state Phase error at $\omega_0$, 3$\omega_0$, 5$\omega_0$, 7$\omega_0$, 9$\omega_0$ | -23.6, -70.1, -118, -160, -168 $\times 10^{-3}$ dB |
| Phase, gain margin | 31.8°, 9.7 dB |

4.7.1 Compensation of Switch Voltage Drop and DC Supply Variations

$u_p$ can be compensated for variations of the $V_{dc}$ so that the state space model and the control performance are not affected by these variations, as given in (4.72).

$$u_p^{\text{comp.}} = u_p V_{dc}^{\text{nom.}} V_{dc}^{\text{est.}}$$ (4.72)

The value of $V_{dc}^{\text{est.}}$ can be easily measured and filtered by the digital controller in an online manner. $V_{dc}^{\text{nom.}}$ is the nominal value of this voltage which is already included in the prediction model. With this compensation, there is no need for adaptation of the prediction model to supply voltage variations. In addition to this, the voltage drops of IGBT and diode switches decrease or increase the voltage supplied to the LC filter dependent on the direction of the current. This affects the tracking performance and the prediction algorithm. It takes some time for the feedback loop
to respond to this abrupt change in the supplied voltage, and therefore, a sudden voltage drop or rise appears in the output voltage at the zero-crossing of the inverter current. A Feedforward compensator can be implemented by sensing the direction of the predicted transformer current, $i_{L_{t-p}}$, and then, compensating the drop or rise by increasing or decreasing the control effort, $u_p$, accordingly. Equation (4.73) shows how $u_p$ must be compensated in order to achieve the desired $u_pV_{dc}$ voltage at the inverter output.

$$u_pV_{dc} = \frac{1}{2} \left\{ \left( \text{sgn}\left(i_{L_{t-p}}\right) + u_p^{\text{comp}} \right) \left(V_{dc} - 2V_{\text{on IGBT}} \right) \right\} - \left\{ \left( \text{sgn}\left(i_{L_{t-p}}\right) - u_p^{\text{comp}} \right) \left(V_{dc} + 2V_{\text{on Diode}} \right) \right\}$$

(4.73)

Equation (4.74) shows the calculated compensated control effort which also includes the DC voltage compensation of (4.72).

$$u_p^{\text{comp}} = u_p V_{dc}^{\text{nom}} + \text{sgn}\left(i_{L_{t-p}}\right) \left(V_{\text{Diode on}} + V_{\text{on IGBT}} \right)$$

(4.74)

### 4.7.2 Adaptation of the Prediction Model to Filter Parameter Variations

In this section, a method is proposed variations in which the estimated or measured values of plant parameters are used in order to adapt the prediction model to filter parameter variations. In this method, the entries of the prediction model matrices in (4.59) are corrected by some correction terms. These terms are obtained with the assumption of small sampling interval such that the exponential function for discretisation can be approximated by the first four terms of its Tylor series as given in (4.75).

$$e^{\hat{A}T_s} \approx 1 + \hat{A}T_s + \hat{A}^2T_s^2 / 2 + \hat{A}^3T_s^3 / 6$$

(4.75)

By applying this approximation to (4.9) and (4.13) and eliminating the negligible terms, the approximated state space matrices in (4.76) are obtained.
\[
\hat{\mathbf{A}}^z \approx \begin{bmatrix}
1 & \frac{-T_s}{L_i} \\
\frac{T_s}{C_f} & 1
\end{bmatrix}, \quad \hat{\mathbf{B}}^z \approx \begin{bmatrix}
\frac{V_{dc}T_s}{nL_i} \\
\frac{V_{dc}T_s^2}{2nL_iC_f}
\end{bmatrix},
\]

\[
\hat{\mathbf{E}}_0^z \approx \begin{bmatrix}
\frac{T_s^2}{3L_iC_f} \\
\frac{T_s}{2C_f}
\end{bmatrix}, \quad \hat{\mathbf{E}}_i^z \approx \begin{bmatrix}
\frac{T_s^2}{6L_iC_f} \\
\frac{T_s}{2C_f}
\end{bmatrix}.
\]

(4.76)

In addition, the approximated feedforward terms are obtained using (4.38), as follows.

\[
F_0 = F_1 \approx k_i / 2
\]

(4.77)

By using the approximated model, the correction terms for entries are obtained as given in (4.78).

\[
\hat{a}_{1,1}^z = \hat{a}_{1,1}^{\text{nom}}, \quad \hat{a}_{1,2}^z = \hat{a}_{1,2}^{\text{nom}}, \quad \frac{L_i^{\text{nom}}}{L_i^{\text{est}}},
\]

\[
\hat{a}_{2,1}^z = \hat{a}_{2,1}^{\text{nom}}, \quad \frac{C_f^{\text{nom}}}{C_f^{\text{est}}}, \quad \hat{a}_{2,2}^z = \hat{a}_{2,2}^{\text{nom}},
\]

\[
\hat{b}_{1,1}^z = \hat{b}_{1,1}^{\text{nom}}, \quad \frac{L_i^{\text{nom}}}{L_i^{\text{est}}}, \quad \hat{b}_{2,1}^z = \hat{b}_{2,1}^{\text{nom}}, \quad \frac{L_i^{\text{nom}}}{L_i^{\text{est}}}, \quad \frac{C_f^{\text{nom}}}{C_f^{\text{est}}},
\]

\[
\hat{c}_{1,1}^z = \hat{c}_{1,1}^{\text{nom}}, \quad \frac{L_i^{\text{nom}}}{L_i^{\text{est}}}, \quad \frac{C_f^{\text{nom}}}{C_f^{\text{est}}}, \quad \hat{c}_{2,1}^z = \hat{c}_{2,1}^{\text{nom}}, \quad \frac{L_i^{\text{nom}}}{L_i^{\text{est}}}, \quad \frac{C_f^{\text{nom}}}{C_f^{\text{est}}},
\]

(4.78)

where \( \hat{c}_{i,j}^z \) denotes the entries for both the \( \hat{\mathbf{E}}_0^z \) and \( \hat{\mathbf{E}}_i^z \). The \( \text{nom} \) index indicates the nominal value of the parameters as already exists in the prediction model, and \( \text{est} \) indicates the measured or estimated values. The DC supply voltage has already been compensated, and therefore, it is excluded from the correction terms.

Figure 4.18 shows the affected frequency range of the open loop Bode plot for the case in Table 4.4 with and without the corrected prediction. With correction the phase margin was increased by 6.4°. The algorithm also tries to return the gain margin to its value before introduced parameter variations and reduces it by 2.3 dB.
In order to implement an online parameter estimation method, the value of $L_l$ and $C_f$ can be estimated by using the sampled current and voltages. $i_{L_l}$ and $v_{C_f}$ are transformed to the virtual synchronous reference frame by $\alpha \rightarrow \alpha'\beta' \rightarrow dq$ transformation for single-phase parameters. It can be performed by SOGI which can provide some filtering. More filtering may be required in order to minimise the transient effects on the estimation. The delay in estimation caused by conversion and filtering does not affect the stability of the system. As Table 4.4 showed, system is still stable with limited parameter variations. The transformation technique can also be made adaptive to frequency variations.

As shown in Chapter 3, even numbered harmonics are present at the output of transformation in addition to the desired DC value, and they adversely affect the parameter estimation. MAF is used at the outputs to eliminate the harmonic content. Since only the even numbered harmonics are present at the output, a window length of equal to half a main voltage period is required. The parameter estimation is, then, performed by (4.79) and (4.80).
Online implementation of this method or other plant estimation algorithms needs some resources of the digital controller and may not be practical. Moreover, because of inaccuracy of voltage and current measurements, and unmeasured parasitic impedances of the filter and inverter, the accuracy of this method is not guaranteed. Therefore, it is assumed that an offline and accurate method estimates the value of these parameters before DVR start of operation.

4.7.3 Adaptation of Feedback and Feedforward Coefficients

When there is a change in the plant parameters, active damping and stability margins can be affected adversely. The state feedback coefficients can be adaptively changed in order to minimise these effects on the control performance. An adaptive method is proposed in which the target of adaptation is to maintain the same damping performance and stability margins regardless of the filter parameter variations. The feedback coefficients of the resonant compensators are neglected from adaptation. The loop frequency response is to a great extent independent of the plant parameters at the frequencies in the vicinity of the resonant frequencies. Therefore, only the current and voltage feedback coefficients, \( k_i \) and \( k_v \), are considered for the adaptation.

The correction terms are obtained by the assumption that the prediction model has been perfectly adapted to parameter variations. Therefore, with the ideally compensated delay, the inner closed loop transfer function of (4.40) can be used. In order to find the correction terms, the approximated state space matrices in (4.76) are replaced in the transfer function equation. Then, the approximated transfer function is obtained in (4.81) by eliminating the negligible terms.
The equation shows that the feedback coefficients must be corrected according to the estimated plant parameters as given in (4.82) such that the damping ratio does not change with parameter variations.

$$
G_{\text{Cf}}^{\text{inner}} \approx \frac{V_{dc}h^2(z+1)/(2nL_fC_f)}{z^2 + \left(-2 + \frac{V_{dc}h}{nL_f}k_f + \frac{V_{dc}h^2}{2nL_fC_f}k_v\right)z + \left(1 - \frac{V_{dc}h}{nL_f}k_f + \frac{V_{dc}h^2}{2nL_fC_f}k_v\right)}
$$

(4.81)

The DC supply voltage has already been compensated, and therefore, it is excluded from the corrections. The correction of feedforward terms is also given in (4.83) which is obtained by using the approximated values in (4.77) and the $k_{iL}$ correction term obtained in (4.82).

$$
k_{iL} = k_{iL}^{\text{nom}} \frac{L_i^{\text{est}}}{L_i^{\text{nom}}},
$$

$$
k_{\text{VFy}} = k_{\text{VFy}}^{\text{nom}} \frac{L_i^{\text{est}}}{L_i^{\text{nom}}} \frac{C_f^{\text{est}}}{C_f^{\text{nom}}}.
$$

(4.82)

For comparison, the open loop Bode diagram of the system with varied plant parameters as the case in Table 4.4 as well as the adapted system with both the feedback coefficient correction and the model correction is plotted in Figure 4.19. It shows an improvement of 13.1° in the phase margin which returns it to 44.9°. The gain margin has also been returned to its value before the introduced parameter variation which is 8.3 dB. Therefore, when these corrections are applied to the control system, the stability of system is improved and stability margins return to the designed values.

In Figure 4.20, bode plots of the closed loop response to disturbance for the case with varied plant parameters and the case with both the adapted prediction model and the adapted feedback and feedforward coefficients are plotted. The plots show that the adaptive method does not necessarily improve the disturbance rejection but tries to return the frequency response to the normal case in which no parameter variations existed. The disturbance rejection for the frequencies below the main frequency is weakened, but it is still high enough for an effective low frequency disturbance rejection.
Figure 4.19 Open loop Bode diagram without (magenta) and with (blue) parameters variations, and with adapted prediction model and feedback coefficients (red)

Figure 4.20 Output closed loop response to disturbance without (magenta) and with (blue) parameter variations, and with adapted prediction model, feedback and feedforward coefficients (red)
4.8 SIMULATION STUDIES

Modelling and Simulation of the DVR system response with block diagram in Figure 4.2 and the control system in Figure 4.16 is performed in PSCAD/EMTDC with the system parameters listed in Table 4.1.

4.8.1 Case 1: Reference Tracking Performance

For the first case, the performance of the control system to a reference input equal to \( V_{C_f}^{\text{max}} \cos(\omega_0 k T_s) s[k] \) without the presence of disturbance is simulated. Figure 4.21(a) shows the reference input as well as the output voltage of the converter, \( v_{Cf} \), illustrating satisfactory transient and steady-state responses with a settling time about one quarter of main cycle. The control effort which is plotted in Figure 4.21(b) shows that the control effort overshoot is inside the linear region.

![Figure 4.21](image)

Figure 4.21 (a) Transient response to the fundamental harmonic reference input, and (b) control effort.
4.8.2 Case 2: Harmonic Reference Tracking Performance

For the second case, the controller performance was observed in the response to an arbitrary input reference containing odd harmonic voltage references up to 9\textsuperscript{th} harmonic. A disturbance current caused by a rectifier load is also injected to the converter. The disturbance current contains high level of odd harmonics. The response is plotted in Figure 4.22. The output voltage, $v_{CF}$, in Figure 4.22(a) tracks the reference with no obvious steady-state error. The small ripple errors in Figure 4.22(b) are the capacitor voltage ripples. The small spikes are caused by the switch voltage drops during current zero-cross as explained in Section 4.7.1. The compensation algorithm has been able to reduce the tracking error during current zero-cross but has not been able to completely eliminate it.

To test the effectiveness of disturbance rejection, the disturbance current is removed from the system and the response is plotted in Figure 4.23. It shows that the tracking error is similar to the case with the presence of disturbance current in Figure 4.22(b). This illustrates the effectiveness of the controller in rejection of disturbance in the output voltage of the converter.
Figure 4.22 (a) Output and reference voltages, and (b) tracking error

Figure 4.23 Tracking error without the presence of disturbance current
4.8.3 Case 3: No Disturbance Feedforward or Loop Delay Compensation

In the third case, the response without applying either disturbance feedforward or loop delay compensation is evaluated. The response with removed disturbance feedforward is plotted in Figure 4.24. The output voltage, $v_c$, in Figure 4.24(a) shows more transient error. The steady-state tracking error in Figure 4.24(b) also shows some harmonic ripples caused by the disturbance harmonics. The amount of current zero-cross spikes have also increased. This illustrates the effectiveness of disturbance feedforward in eliminating the harmonic contents from the output voltage.

Figure 4.24(a) Output and reference voltages, and (b) tracking error without disturbance feedforward

Figure 4.25 shows the response when the delay compensation algorithm is not applied. The tracking error in Figure 4.25(b) has increased considerably in both the transient and steady-state conditions. This is caused by the high bandwidth of the
system. The variations of the currents and voltages during the loop delay of one sampling interval is so high that considering fixed values for the current and voltages leads to inaccurate calculation of feedback control values. This increases the ripple errors and reduces the stability of the system.

![Figure 4.25(a) Output and reference voltages, and (b) tracking error without loop delay compensation](image)

**Figure 4.25(a) Output and reference voltages, and (b) tracking error without loop delay compensation**

### 4.8.4 Case 4: Adaptive Algorithm Performance

In the fourth case, performance of the adaptive algorithm is studied. Tracking error in response to the arbitrary reference voltage when plant parameters are varied as the case in Table 4.4 is plotted in Figure 4.26(a). In addition, the tracking error for the adapted control system when the model adaptation, feedback coefficient adaptation and feedforward coefficient adaptation are applied is plotted in Figure 4.26(b). The results show that the system is robust to small parameter
variations and the tracking error has not changed noticeably. Thus, when the adaptation is applied, no considerable improvement is observed in the response.

Since the effectiveness of the adaptation method in stabilising the system cannot be clearly seen in Figure 4.26, a case with extreme plant parameter variations is simulated. Both the values of inductance and capacitance were dropped by 40%. Figure 4.27 shows that without adaptation the output voltage, $v_{Ch}$, has high frequency ripples and the tendency to instability. The phase margin in this case is about 2.5°. However, the tracking error of the adapted system in Figure 4.28 shows a stable response with a decreased tracking error. This proves the effectiveness of the proposed adaptive algorithm in stabilising the system and reducing the tracking error.
4.8.5 Case 5: Load Disconnection and Reconnection Performance

The fifth case illustrates the response to the whole grid load disconnection and reconnection in Figure 4.29. The load is discounted at 135 ms. A high voltage ripple is generated which is caused by the slow operation of the feedback controller in response to the abrupt change. The disturbance feedforward operation also increases the overshoot, because the transient response has not been considered in the design of the feedforward compensator. Nonetheless, the response time is short and the voltage overshoot ripples disappear after about 3 ms, and the voltage settles back to the reference after about 11 ms. In addition, the response to the load reconnection at 160 ms does not show any considerable transient fluctuations.
Figure 4.28 Response with adaptation to the extreme parameter variations, (a) output voltage, and (b) tracking error

Figure 4.29 Response to a load disconnection at 135 ms and reconnection at 160 ms
4.9 EXPERIMENTAL STUDIES

In order to test the feasibility and performance of the control algorithm, some Hardware-in-The-Loop (HIL) tests are performed. The control algorithm is implemented using TI TMS320F28335 DSP microcontroller and tested using Typhoon HIL. An introductory description for the operation of this device and its DSP interfacing is provided in Appendix A. This device emulates the behaviour of the modelled DVR system in Figure 4.30, and simulated current and voltage signals are fed back to analogue inputs (AI) of DSP via analogue outputs (AO) of the device. The feedback and control signals are as indicated in Figure 4.2. The acquired signals by DSP are converted to digital values using its ADC module. The programmed control algorithm generates the control effort signal which is translated to PWM signals commanded to digital inputs (DI) of Typhoon to control the state of IGBT switches.

![Figure 4.30 DVR system emulation model in Typhoon HIL schematic editor](image)

4.9.1 Case 1: Harmonic Reference Tracking Performance

The steady-state response to the arbitrary reference input for the realised control algorithm which was already simulated in Figure 4.22(a) is verified in Figure 4.31. The output voltage, $v_{Cy}$, acquired for one main cycle shows that it is able to follow the reference input in presence of harmonics in the disturbance current. The plot also shows the transformer current and its switching ripples.
The response for the case without both the delay compensation and the disturbance prediction shows an unstable behaviour. However the simulation case in Figure 4.25 only showed the tendency to instability. The instability observed in the implementation is caused by the reduced phase margin as discussed in Section 4.6 and the nonlinearity in signal acquisition introduced by saturation of AOs of Typhoon. This is caused by the limited voltage range of AOs of the device which resembles the sensor saturation. Therefore, the results in Figure 4.31 show the effectiveness of the delay compensation method in stabilising the control system.

### 4.9.2 Case 2: Adaptive Algorithm Performance

In this case, the operation of the proposed adaptive control and prediction method is observed. Figure 4.32 shows the output voltage, $v_{Cf}$, and transformer current in presence of extreme parameter variations of -40%, as previously simulated in Figure 4.27. The increased current and voltage ripples and tendency to instability caused by prediction inaccuracies can be observed in the plot.

After applying the adaptive algorithm, the response is plotted in Figure 4.33. It shows that the adaptive control algorithm has been able to improve the stability of the control system and reduce the current and voltage ripples compared to
Figure 4.32. The tracking error is also decreased. The experimental results prove the effectiveness and feasibility of the proposed adaptive algorithm.

Figure 4.32 Response in presence of extreme parameter variations

Figure 4.33 Response in presence of extreme parameter variations and applied adaptive algorithm

Figure 4.33 Response in presence of extreme parameter variations and applied adaptive algorithm
4.10 CONCLUSIONS

The main disadvantage of series compensation which is its protection issues was surveyed and the suggested solutions in literature were provided. Then, a procedure for the design of the DVR converter is introduced. Firstly, the LC filter was designed in order to limit the current and voltage ripples and losses of the filter. Then, a control algorithm based on IMP for reference tracking of the converter was designed. The algorithm was extended by using stacked compensators in order to be able to track the harmonic references as well. Moreover, an improved pole placement method was proposed in order to obtain the feedback coefficients of the control system. It was also shown that the disturbance feedforward is an effective method to improve the disturbance rejection of the control system. The simulation and implementation results showed the effectiveness of the control algorithm in reference tracking and disturbance rejection.

In addition, a model-based prediction algorithm was proposed in order to compensate the loop delay introduced by the computation time of the digital controller. With prediction, control design is performed without considering the delay which simplifies the control design procedure. Because the used prediction method is a model-based one, the algorithm was improved by a proposed algorithm for adaptation of prediction model to plant parameter variations. Moreover, an adaptation method for feedback coefficients were also proposed to maintain the stability margins of the control loop in presence of parameter variations. The Bode plots and simulation results showed the effectiveness of the adaptive algorithms.

The designed control algorithm will be used for the control of DVR in the next chapter in which a reference input is generated by a voltage quality improvement algorithm and is tracked by the converter output. The stable and effective operation of the control algorithm in reference tracking and disturbance rejection is the key factor in successful usage of DVR in networks.
In this chapter, the converter designed in the Chapter 4 is used as a series compensator for the application of grid voltage regulation and quality improvement. In this application, an improved optimisation algorithm using clustered load levels of network buses is proposed in order to determine the location and sizing of Dynamic Voltage Restorer (DVR) in a network such that the minimum required DVR rating is obtained. The optimisation process also defines an optimum tap setting for distribution transformer. In this approach, one of the optimisation objectives is to achieve minimum voltage deviations in the network by considering the static operation of the network at different clustered load levels.

Apart from optimisation, in this chapter, a regulation algorithm is also proposed in order to achieve an online and appropriate voltage regulation in the network while loads and generations are changing. This algorithm does not need any communication links between buses and DVR for obtaining the online network information. For this purpose, a value which is referred to as equivalent line impedance (ELI) is defined. The local measured current and voltage at the DVR location along with the calculated equivalent line impedance are used to estimate the average voltage deviation in DVR downstream network and to calculate the required amount of compensation.

The idea is then extended for compensation of harmonic distortion in bus voltages, and thus, equivalent line impedances for harmonic frequencies are obtained so that the compensation can be performed without the need for communication. In addition, the shunt compensation using Distribution Static Synchronous Compensator (D-STATCOM) is also considered for optimisation in order to compare the effectiveness of series and shunt compensation methods.

5.1 GRID VOLTAGE REGULATION

The traditional design of low voltage (LV) residential grids does not consider the impact of renewable energy resources, and usually, a fixed tap setting between 1.02 and 1.05 pu on the secondary side of distribution transformers is set to
overcome the high voltage drops during peak load periods. However, high penetration of Distributed Generation (DG) units changes the operation of networks in an adverse manner. To illustrate the problem, the simplified equivalent circuit of an LV grid is considered as depicted in Figure 5.1.

![Figure 5.1 Equivalent circuit of the traditional LV grid](image)

In this figure, $V_s$ is the RMS phasor voltage at the secondary side of distribution transformer considered with zero phase angle, $V_e$ is the RMS phasor of equivalent bus voltage, $Z_e$ equals to $R_e + jX_e$ and is the equivalent line impedance of the network, and $P_D$ and $Q_D$ are the total equivalent active and reactive loads of the LV grid. The voltage deviation can be approximated as follows [4].

$$\Delta V = V_e - V_s \approx -\frac{R_e P_D + X_e Q_D}{V_e}$$

Values of $R_e$ and $X_e$ are fixed, and values of $P_D$ and $Q_D$ are uncontrollable in the traditional network operation. Therefore, the only way to regulate and keep $V_e$ in the permissible range is to vary $V_s$. As noted before, a tap on the secondary side of the distribution transformer is fixed between 1.02-1.05 pu to regulate this voltage. Once the tap setting is changed, it remains fixed and will not be changed for a long period of time such as a season. By introducing renewable energy units such as PV resources into residential grids, the power flow changes. Figure 5.2 is an equivalent model which shows the voltage issue of LV grids when renewable generation is added to the network. In this case, $V_e$ can be approximated as given in (5.2).

![Figure 5.2 Equivalent circuit of the LV grid with renewable energy units](image)

$$\Delta V = V_e - V_s \approx -\frac{R_e (P_G - P_D) + X_e (Q_G - Q_D)}{V_e},$$

(5.2)
where $P_G$ and $Q_G$ are the total equivalent generated active and reactive power of photovoltaics (PV). Based on the electricity network standards, PV inverters have been traditionally required to operate with a power factor close to unity, and therefore, the value of $Q_G$ is too low to influence the voltage levels as required. It can be observed from the equation that if the equivalent generated power exceeds the equivalent load, $V_e$ may rise and pass the standard voltage limit forcing a disconnection of renewable energy sources as well as adverse effect on sensitive loads. By changing any of the parameters in equation (5.2), i.e. $R_e$, $X_e$, $P_D$, $P_G$ or $V_s$, the voltage rise issue could be controlled. In the traditional operation of LV networks, these parameters cannot be controlled. However, thanks to the paradigm of the smart grid for electricity networks, as a lot of research work has been reported on the use of these parameters to deal with voltage regulation issue in distribution networks. To reduce the value of $R_e$, line can be upgraded to increase the cross section area of cables [131]. To increase the value of $P_D$ and reduce the voltage, the smart controllable devices can be coordinated in the residential grid [132]. Moreover, PV active power curtailment and storage units can be utilised to control the PV injection, $P_G$ [1, 98]. However, parameter $V_s$ has not been considered in the literature for improving the voltage quality in LV grids. A series connected Voltage Source Converter (VSC) such as a DVR at the secondary of distribution transformer can be used in order to adjust the $V_s$ in an online manner so that the required regulation is achieved. This structure is derived from the idea of On-Load Tap-Changer (OLTC) in distribution networks but with the benefit of online and continuous regulation. DVR can shift $V_s$ upward or downward, and thereby, bus voltages of the downstream network are shifted as well. Using this method, the regulation influences all bus voltages in the network. However, it may be not required to shift all the bus voltages in order to achieve a desired voltage control and regulation all over the network.

For illustration, a uniform single-line distribution network with uniform loadings and generations is considered in Figure 5.3. The farthest bus from the supply is subject to the highest voltage fluctuations compared to the other buses. This is because the highest impedance up to the supply voltage is seen from this point. Further to this, uniform demand and generation of other buses causes additional voltage rise and drop at this point. Therefore, the further this bus is from the source, the more voltage deviations can be observed at the bus. If $V_s$ is shifted by a DVR to regulate the badly
affected buses, there may be a need to have a high compensation voltage which may lead to high voltage deviations or even crossing the standard voltage limits at buses close to the DVR location. This issue can be overcome by optimal placement of the DVR in a branch where it regulates bus voltages of its downstream network while desired maximum voltage deviations are achieved along the network.

In the proposed structure for regulation of LV grids, the DVR is connected in series to a branch in an optimised location as shown in Figure 5.4. As LV grids are usually unbalanced, it is proposed that this structure should be applied per phase basis. However, a three-phase structure can also be used as discussed in Section 5.9. In this structure, \( V_{1s} \) is the voltage at the upstream side of DVR, \( V_{2s} \) is the voltage at the downstream side of DVR, and \( I_d \) is the grid current flowing through the DVR converter.

The downstream network is replaced by an equivalent circuit which is defined in Section 5.4, and the aim is to regulate the equivalent average voltage of the network, \( V_e \), to a pre-specified value. There are two possible approaches for achieving this objective. In the first approach, bus voltages can be monitored and sent to the DVR controller as control variables. This approach needs communication between buses and DVR controller which is subject to communication failure. The second approach,
as proposed in this thesis, is to approximate the average voltage of DVR downstream buses as $V_e$ so as to be able to regulate it, and thus, minimise or limit the average voltage deviation without the need for any communication link.

A sample non-uniform 6-bus network as depicted in Figure 5.5 is considered for optimisation and simulation. Each bus consists of constant power, constant current and constant impedance loads as well as constant power generation.

![Figure 5.5 Sample non-uniform 6-bus network](image)

In LV networks, load and generation profile during a year for all the buses can be obtained by monitoring or using billing information. Based on the obtained profile, a descending Load Duration Curve (LDC) can be defined for each bus which illustrates correlated values of demand and generation and their corresponding duration in the one year period. Then, a clustering method is applied to the LDC to find average clustered values and their duration (probability of occurrence) in the period for each bus. This approach effectively reduces the optimisation computations while retaining a high level of accuracy. Figure 5.6 shows an example for the $i$-th bus in which four clustered load levels with different durations, $P(L_j)$, are obtained. The clustering technique produces the same cluster durations for all buses.

![Figure 5.6 Example of clustering applied to LDC for $i$-th bus](image)
The proposed algorithms in this chapter can be applied to large networks as well. These networks can be simplified to smaller ones with reduced number of buses. This can significantly reduce the computational load required for optimisation process and improve the convergency to a global optimum solution. For this purpose, large downstream networks branched from the main network can be replaced with their equivalent network. Therefore, the whole branched network is simplified to its equivalent line impedance plus its equivalent load with clustered load levels. For example, the branch 5 and the bus 6 as well as the branch 4 and the bus 5 could be the equivalent networks for two large downstream networks branching from bus 3 and bus 4, respectively.

5.2 STATIC LOAD FLOW ANALYSIS WITH DVR

Network load flow analysis is required in order to obtain bus voltages and branch currents as part of optimisation process. For load flow analysis for each set of clustered load levels, the nominal apparent power injection of \( i \)-th bus with 1 pu bus voltage is considered, as given in (5.3), using the provided network data.

\[
S_i^{\text{nom}} = S_{di}^{\text{nom}} - S_{gi}^{\text{nom}} = \left( P_{di}^{\text{nom}} + jQ_{di}^{\text{nom}} \right) - P_{gi}^{\text{nom}}, \quad i = 2 \ldots N \quad (5.3)
\]

The calculated apparent power is valid for constant power buses. For inclusion of different types of injections at buses, including constant current and constant impedance load as well as constant power load and PV generation, the apparent power at each bus needs to be recalculated based on the calculated bus voltage magnitude as follows.

\[
S_i = \left( \alpha_i^Z \left( V_i \right)^2 + \alpha_i^V V_i + \alpha_i^{PQ} \right) S_{di}^{\text{nom}} - S_{gi}^{\text{nom}}, \quad \alpha_i^Z, \alpha_i^V, \alpha_i^{PQ}
\]

where \( \alpha_i^Z \) is the share of constant impedance load in the nominal apparent power demand for \( i \)-th bus, \( \alpha_i^V \) is the share of constant current load, and \( \alpha_i^{PQ} \) is the share of constant power load.

For the load flow analysis of a typical network, (5.5) to (5.9) are performed iteratively based on direct load flow analysis proposed in [133, 134]. This method is faster than other load flow analysis methods, and therefore, it can reduce the convergence time of iterative optimisation techniques.
\[ S_i^k = \left( \alpha_i^2 (V_i) + \alpha_i V_i + \alpha_i^{PQ} \right) S_{gi}^{nom} - S_{gi}^{nom}, \quad 2 \leq i \leq 6, \quad (5.5) \]

\[ T_i^k = \left( \frac{S_i^k}{\gamma_i^k} \right)^*, \quad 2 \leq i \leq 6, \quad (5.6) \]

\[ B^k = [BIBC]^t^k, \quad (5.7) \]

\[ \Delta V^k = -[BCBV]B^k = -[DLF]^t^k, \quad (5.8) \]

\[ V^k = V_1 + \Delta V^k, \quad (5.9) \]

where \( k \) is the iteration number, \( S_i \) is the apparent power injection of \( i \)-th bus, \( T_i \) is the bus injection phasor current, \( \gamma_i \) is the bus phasor voltage, \( \Delta V \) is the bus voltage deviation matrix, and \( V_1 \) is an \( N\times1 \) dimensional matrix with the slack bus voltage of \( \gamma_i \) as entries which is defined by the distribution transformer tap setting. \( B \) in (5.7) is the branch current matrix, \( I \) is the bus current matrix, and \( [BIBC] \) is the bus injection to branch current matrix. The relationship between bus current injections and branch currents given in (5.7) is expressed as follows for the 6-bus network.

\[
\begin{bmatrix}
[ B_1 ] & [ 1 1 1 1 1 ] [ T_1 ] \\
B_2 & [ 0 1 1 1 ] [ T_2 ] \\
B_3 & [ 0 0 1 ] [ T_3 ] \\
B_4 & [ 0 0 0 1 ] [ T_4 ] \\
B_5 & [ 0 0 0 0 1 ] [ T_5 ]
\end{bmatrix}
= \begin{bmatrix}
T_1 \\
T_2 \\
T_3 \\
T_4 \\
T_5
\end{bmatrix}
\quad (5.10)
\]

In addition, \( \Delta V \) in (5.8) is the bus voltage deviation matrix, and \([BCBV]\) is the branch current to bus voltage matrix calculated as follows.

\[
[BCBV] = [BIBC]^T Z. \quad (5.11)
\]

\( Z \) is the branch impedance matrix which is diagonal matrix containing branch impedances as the main diagonal entries. Therefore, equation (5.8) can be expressed as follows using (5.11).
Furthermore, $[\text{DLF}]$ in (5.8) is the distribution load flow matrix obtained as follows.

$$[\text{DLF}] = [\text{BCBV}][\text{BIBC}] \quad (5.13)$$

The typical load flow analysis must be modified, if DVR is placed in series with the $b$-th branch (at $(b+1)$-th bus) by entering the effect of the series DVR voltage on the network. The buses at the downstream side of DVR are affected by DVR voltage. Therefore, this voltage is added to the downstream bus voltage deviations in (5.8), and bus voltages are calculated as follows.

$$\Delta V^k = -[\text{DLF}] \times I^k + V_{DVR}^k \quad (5.14)$$

$$V^k = V_i + \Delta V^k \quad (5.15)$$

Downstream buses can be marked by using the $b$-th row of BIBC matrix in (5.10), and thus, $V_{DVR}$ is calculated as,

$$V_{DVR}^k = V_{rms}^{DVR} \angle \theta_{DVR}^k \cdot \begin{bmatrix} \text{BIBC}_{b,1} & \cdots & \text{BIBC}_{b,N-1} \end{bmatrix}^T. \quad (5.16)$$

As discussed in Section 5.5, in the case when no active power injection by DVR is required, the phase angle of DVR voltage, $\theta_{DVR}$, is obtained in each iteration using the phase angle of DVR branch current, $B_b$, as given in (5.17). The $90^\circ$ phase shift eliminates active power injection by DVR.

$$\theta_{DVR}^k = \theta_{B_b} + \pi/2 \quad (5.17)$$

The power rating of DVR converter can also be calculated as follows.

$$S_{DVR} = V_{DVR} B_b \quad (5.18)$$

### 5.2.1 Harmonic Load Flow Analysis

Calculation of Total Harmonic Distortion (THD) of bus voltages requires information about the level of distortion all over the network. This information can
be used by the optimisation algorithm in order to obtain a desired location and rating for the DVR in order to minimise the average THD all over the network.

The analysis must be performed for each selected harmonic order, $h$, to obtain the corresponding voltage distortion by that harmonic frequency. The analysis is similar to the fundamental frequency analysis with minor modifications. The \([{\text{BHCBHV}}]\) (Branch Harmonic Current to Bus Harmonic Voltage) and \([{\text{HLF}}]\) (Harmonic Load Flow) matrices use the values of branch impedances for each harmonic frequency, and therefore, branch reactance must be multiplied by the harmonic order as follows.

$$Z_h = \text{Re}(Z) + h \cdot \text{Im}(Z), \quad h = 3, 5, 7\ldots$$  \hspace{1cm} (5.19)

$$[{\text{BHCBHV}}]_h = [{\text{BIBC}}]^T Z_h$$  \hspace{1cm} (5.20)

$$[{\text{HLF}}]_h = [{\text{BHCBHV}}]_h [{\text{BIBC}}]$$  \hspace{1cm} (5.21)

For short lines, low order harmonics and overhead cables, the series impedance provides a good representation of the line. Otherwise, the inclusion of line shunt capacitance is necessary [135]. The Π representation of branches can be used for load flow analysis in which the branch line capacitance is halved and placed at its two terminal buses. This yields equation (5.22) which represents the total admittance of equivalent line capacitances at each bus.

$$\begin{bmatrix}
Y_{2C} \\
Y_{3C} \\
Y_{4C} \\
Y_{5C} \\
Y_{6C}
\end{bmatrix} =
\begin{bmatrix}
\frac{(Y_{12}^C + Y_{23}^C)}{2} \\
\frac{(Y_{23}^C + Y_{34}^C + Y_{36}^C)}{2} \\
\frac{(Y_{34}^C + Y_{45}^C)}{2} \\
Y_{45}^C/2 \\
Y_{36}^C/2
\end{bmatrix}$$  \hspace{1cm} (5.22)

The analysis is performed iteratively using (5.23) to (5.27) and considering zero value for harmonic content of the source voltage, $V_{1,h}$, and no harmonic current generation by PV inverters. Additionally, the reactive power injection at buses by equivalent line capacitors is also included in the total bus injection.

$$S_{i,h}^k = \left(\alpha_i^Z (V_{i,h}^k)^2 + \alpha_i^V V_{i,h}^k + \alpha_i^{\text{PQ}}\right) S_{di,h}^{\text{nom.}} - jhY_i^C (V_{i,h}^k)^2 \quad h = 3, 5, 7\ldots , \hspace{1cm} (5.23)$$
\[ I_{i,h}^k = \left( \frac{S_{i,h}^k}{V_{i,h}^k} \right)^*, \quad (5.24) \]

\[ B_h^k = [\text{BIBC}] I_h^k, \quad (5.25) \]

\[ \Delta V_h^k = -[\text{HLF}_h] I_h^k + V_{DVR,h}^k, \quad (5.26) \]

\[ V_h^k = \Delta V_h^k, \quad (5.27) \]

where \( S_{i,h} \) is the bus power injection for the \( h \)-th harmonic order, and \( V_{DVR,h} \) is the matrix of DVR RMS harmonic voltage on the affected buses calculated using (5.16) for each harmonic order. In addition, THD for each bus for the selected harmonics is calculated as follows.

\[ \text{THD}_i = \sqrt{\sum_{h=3,5,7,9} \frac{V_{i,h}^2}{V_i^2}} \times 100\% \quad (5.28) \]

The power injection of DVR for each harmonic order is calculated using the magnitude of harmonic content of DVR branch current, \( B_{b,h} \), as follows.

\[ S_{DVR,h} = V_{DVR,h} B_{b,h}^* \quad (5.29) \]

### 5.3 OPTIMAL PLACEMENT AND SIZING OF DVR

To achieve the best performance of DVR operation, an optimal placement and sizing algorithm is developed using the hybrid of constricted Particle Swarm Optimisation (PSO) and Genetic Algorithm (GA) crossover explained in Section 2.3.1. The algorithm finds the best location and voltage of DVR in order to minimise the rating while a desired voltage regulation and quality all over the network in all loading conditions is satisfied. For this purpose, an objective function is defined and its minimum in the \( n \)-dimensional decision variable hyperspace is found by the algorithm.

For a better optimisation, the tap of distribution transformer is also considered as an input parameter for optimisation as well as the location and voltage of DVR. Different tap settings result in different optimisation results and may improve the rating of DVR. Since all clustered load levels are considered for optimisation, the
optimised results are valid throughout a year and the tap setting does not need any further adjustment.

Particle vector includes the decision variables of optimisation which are two discrete and four real values including tap setting of distribution transformer \((T)\), DVR location at bus number \((b+1)\), and DVR voltages in different load levels \(V_{DVR}\), as illustrated in Figure 5.7. These variables form the six dimensional vector of particle.

\[
X_1 = T, \quad X_2 = (b+1), \quad x_3 = V_{DVR}^{L_1}, \quad x_4 = V_{DVR}^{L_2}, \quad x_5 = V_{DVR}^{L_3}, \quad x_6 = V_{DVR}^{L_4}
\]

Figure 5.7 Particle vector structure and included optimisation variables

‘Bus number’ and ‘Tap setting’ are the two discrete variables. In order to use the rounding function in (2.12) for the tap setting, the variable is considered as an integer variable in the optimisation process, and therefore, is multiplied by tap adjustment of 2.5% for load flow analysis as follows.

\[
V_1 = 1 + 2.5\% \times T \quad (5.30)
\]

All optimisation variables are constrained based on the network data and voltage limit of the designed DVR in the previous chapter given in Table 5.1. In addition, the DVR is assumed to be injecting only reactive power, and therefore, (5.17) is used for calculation of DVR voltage phase angle.

Table 5.1 Constraints of optimisation variables

<table>
<thead>
<tr>
<th>Bus Number ((b+1))</th>
<th>2, 3, 4, 5, 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tap Setting ((T))</td>
<td>-2, -1, 0, 1, 2</td>
</tr>
<tr>
<td>Tap Adjustment</td>
<td>±2.5%</td>
</tr>
<tr>
<td>DVR Voltage ((V_{DVR}))</td>
<td>-0.21…0…0.21 pu (RMS)</td>
</tr>
<tr>
<td>Load Level ((L_j))</td>
<td>1, 2, 3, 4</td>
</tr>
</tbody>
</table>

The average deviation of bus voltages in the network from a reference voltage, \(V_e^{ref}\), which is typically 1 pu, can be calculated by (5.31) which also includes the duration of clustered load levels, \(P(L_j)\).

\[
\Delta V_e = \sum_{j=1}^{LL} \left[ P(L_j) \sqrt{\frac{1}{N} \sum_{i=2}^{N} \left( \frac{V_i^j - V_e^{ref}}{V_e^{ref}} \right)^2} \right] \times 100\% \quad (5.31)
\]
$V_{i,j}$ is the voltage magnitude of $i$-th bus in the $j$-th clustered load level. $N$ is the number of buses in the network, $LL$ is the number of cluster sets, and $P(L_j)$ is the duration of each cluster.

The duration of clustered load levels has a weighting effect on the calculation of average deviation such that the clustered load levels with higher duration have more influence on the calculation of average deviation. The objective function can be defined as the argmin of average voltage deviation cost function as given in (5.32). The constraints

$$\{X_1, X_2, x_3, \cdots\} = \arg \min \left[ \Delta V_c \left(X_1, X_2, x_3, \cdots\right) \right],$$

Subject to:

$$V_{lo} \leq V_{i,j} \leq V_{hi}, \quad i = 2\ldots N, \quad j = 1\ldots LL$$

The optimisation for this objective function may have more than one solution, and the best option can be selected based on other design criteria such as DVR rating and power loss of the network. The load flow analysis gives the necessary information for calculating the total network loss. The average power loss can be calculated using the calculated bus currents and provided line resistances as well as the duration of clustered load levels, as given in (5.33).

$$P_{loss} = \mathbf{R} \times \sum_{j=1}^{LL} \left( P(L_j) \begin{bmatrix} (B_{1,j})^2 & \cdots & (B_{N-1,j})^2 \end{bmatrix}^T \right),$$

where $B_{i,j}$ is the magnitude of $i$-th branch current calculated for $j$-th clustered load level using (5.10), and $\mathbf{R}$ is the vector of branch resistances as given in (5.34).

$$\mathbf{R} = \begin{bmatrix} R_1 & \cdots & R_{N-1} \end{bmatrix}$$

By having this information, the optimisation can also be performed for the minimum power loss of the grid so that the results for this optimisation target can be compared to the other ones. In order to optimise for the network loss, the objective function and constraints in (5.35) with the grid power loss as the cost function is used.

$$\{X_1, X_2, x_3, \cdots\} = \arg \min \left[ P_{loss} \left(X_1, X_2, x_3, \cdots\right) \right],$$

Subject to:

$$V_{lo} \leq V_{i,j} \leq V_{hi}, \quad i = 2\ldots N, \quad j = 1\ldots LL$$
Objective function can also be defined to obtain minimum required DVR rating which was already calculated by (5.18). Since for different clustered load levels different ratings are calculated, the maximum of calculated ratings among the different load levels is used as the cost function as follows, where $S_{DVR}^j$ is the calculated DVR rating in the $j$-th load level.

$$S_{DVR}^{\text{max}} = \max \left( S_{DVR}^j \right), \quad j = 1 \ldots LL,$$

$$\{X_1, X_2, x_3, \ldots\} = \arg \min \left[ S_{DVR}^{\text{max}} \left( X_1, X_2, x_3, \ldots \right) \right],$$

Subject to:

$$V_{lo} \leq V_i^j \leq V_{hi}, \quad i = 2 \ldots N, \ j = 1 \ldots LL$$

The obtained rating is calculated based on the obtained clustered load levels which are average values. Therefore, a margin for the rating must be considered because of the network power fluctuations. The future demand growth and increasing PV penetration may also compel to further increase the margin.

The minimisation of THD can also be considered as an objective but has not been considered in the optimisation. However, an online method for compensation of harmonic content is proposed in Section 5.6. The average THD of network can be obtained by using (5.28) as given in (5.38), and consequently, the objective function can then be defined as given in (5.39).

$$THD_e = \sum_{j=1}^{LL} \left[ P \left( L_j \right) \frac{1}{N} \sum_{i=2}^{N} THD_i \right]$$

$$\{X_1, X_2, x_3, \ldots\} = \arg \min \left[ THD_e \left( X_1, X_2, x_3, \ldots \right) \right]$$

Subject to:

$$V_{lo} \leq V_i^j \leq V_{hi}, \quad i = 2 \ldots N, \ j = 1 \ldots LL$$

In order to keep bus voltages within the constraints, a high cost penalty value is added to the objective functions, if any grid voltage limit violation occurs in any clustered load level. Thus, the optimisation algorithm tries to keep the bus voltages within the boundaries, and the objective of bus voltage regulation to remain within the boundaries is also achieved with any of the objective functions.

Furthermore, by including different criteria in the objective functions, a multi-objective optimisation problem can be defined in order to minimise the total cost of
two or more objectives or to have a balance between objectives. The costs are therefore weighted to make a multi-objective cost function, $J$, as given in (5.40), and the weight of each cost, $w_x$, is adjusted to reflect its importance [136]. Thus, the objective function is obtained as given in (5.41).

$$J = w_D \Delta V_e + w_L P_{loss} + w_{\text{max}} S_{\text{DVR}} + w_H THD_e$$  \hspace{1cm} (5.40)

$$\{X_1, X_2, x_3, \ldots\} = \arg \min \left[ J \left( X_1, X_2, x_3, \ldots \right) \right]$$

**Subject to:**

$$V_{lo} \leq V_i^j \leq V_{hi}, \quad i = 2\ldots N, \ j = 1\ldots LL$$  \hspace{1cm} (5.41)

The optimisation flowchart is depicted in Figure 5.8 and explained as follows.

In the initialisation process, a population of particles is generated in which each particle contains random values for optimisation variables. An initial random velocity is also defined for each particle. Each particle represents a candidate solution for the optimisation problem. For calculating the objective function, a load flow analysis is performed for each particle’s vector values as explained in Section 5.2. The network configuration for load flow analysis which include the transformer tap setting, DVR location and DVR voltage, are given by the particle vector. The analysis is performed for all the clustered load levels of the network using the corresponding DVR voltage given by the particle. Then, the objective function is calculated for each particle using the results of the load flow analyses. The constraints in (5.32) are also checked, and if a violation occurs in any of the buses and in any clustered load level, objective function is penalised by adding a high cost value to the function. Then, the estimated objective function value for each particle is used to find the particle’s best and the global best in the optimisation hyperspace. Afterwards, the population is updated by the velocity of each particle which is calculated based on the best solution seen so far by that particle and the best global solution among all particles. Then, a set of parents is randomly selected from the population for performing position and velocity crossover. The generated children replace the parents and the program proceeds to the next iteration. This procedure is continued until convergence is achieved.
5.4 CALCULATION OF EQUIVALENT LINE IMPEDANCE

The optimisation finds the optimised DVR voltage magnitudes, as part of decision variables, in all the clustered load levels which are defined based on average loading of buses. The loads, however, are variable and fluctuate as time passes. Therefore, an estimation of grid voltage deviations must be performed so that DVR voltage is adjusted by its controller to regulate bus voltages in an online manner. The online information available for DVR controller is the local current, $I_d$, and local upstream and downstream voltages, $V_{s1}$ and $V_{s2}$. Therefore, by defining an equivalent line impedance (ELI) for the downstream network which resembles the line impedance, $Z_e$, in Figure 5.2 and equation (5.2), the equivalent voltage deviation for $M$ number of downstream buses can be calculated by averaging voltage deviations of these buses as given in (5.42). Since DVR cannot affect the upstream network, only the downstream network is considered for calculation of ELI.

$$\Delta V_{\text{downstream}}^e (t) = \frac{1}{M} \sum \Delta V_i (t) = Z_e (t) I_d (t)$$  \hspace{1cm} (5.42)

The equation shows that ELI is a time varying parameter. However, an average value for this parameter can be calculated based on the obtained clustered load levels. This
estimated value can be used for estimation of average voltage deviation in all loading and generation conditions. This estimation is more accurate, if buses have more uniform power injection variations as time passes.

For calculation of a constant ELI, considering (5.42), the average of voltage deviations of downstream buses from the bus voltage at DVR location needs to be calculated. For instance, for the uniform single-line network in Figure 5.3, the average voltage deviation for bus number 2 up to the end of the line and the ELI seen from DVR location can be calculated as follows.

\[
Z_c = \frac{1}{M} \sum_{j=1}^{N} \frac{\Delta V_j(t)}{I_j(t)} = \frac{1}{N-1} \sum_{j=1}^{N} \Delta V_j = \frac{\sum_{j=1}^{N} \sum_{i=j}^{N-1} \frac{I_j}{N-1} Z_b}{(N-1) I_j} \tag{5.43}
\]

For a general network with non-uniform clustered load levels, different types of loads and with different branch impedances, the load flow analysis data can be used for obtaining the average voltage deviation. The duration of clustered load levels is also used as a weighting factor for calculation of ELI. Thus, apart from load values, the regulation algorithm is more inclined for regulation of clustered load levels with higher probability of occurrence. By using [BIBC] matrix, downstream buses of DVR, including DVR bus, can be marked and included in the calculation of average voltage deviation. ELI is, therefore, calculated as follows using the load flow analysis results for optimised network configuration and all the clustered load levels.

\[
Z_c = \sum_{j=1}^{L} \frac{1}{M} P(L_j) \frac{BIBC_{b,1} \cdots BIBC_{b,N-1}}{B_{b,i}} \left[ V_{b+1} - V_{i} \right] \tag{5.44}
\]

\( V_{b+1} \) is an \( N-1 \times 1 \) dimensional matrix with entries equal to bus phasor voltage at DVR location, \( V_{b+1} \), and \( V \) is the bus phasor voltage matrix. \( B_{b,i} \) is the branch phasor current at DVR location which was already noted as \( I_d \), and \( M \) is the number of downstream buses which is equal to the number of non-zero entries of \( b \)-th row of BIBC matrix. The ELI is used by DVR controller for estimation of the average voltage deviation of downstream network which is to be regulated.

It must be noted that DVR cannot affect upstream bus voltages. However, the developed optimal placement can find the best DVR location for minimum network voltage deviations including both upstream and downstream bus voltages. Therefore,
by regulating only the downstream network with the online regulation algorithm, the minimisation of voltage deviations all over the network can also be achieved.

Apart from this, current residential networks generally rely on PV for power injection. Therefore, during the day, high voltage rises are seen all over the network and high voltage drops are encountered during the evening. This implies that a similar voltage profile exists for all buses and regulation of the network average voltage is effective in regulation of bus voltages all over the network. However, if the network has very different characteristics in different areas such that while having high voltage rise in some areas, high voltage drop is seen in some other areas, the network can be divided into sections and a DVR is used at the upstream end of each section. Hence, the average voltage of each section with similar bus characteristics is regulated, and thus, bus voltages all over the network are regulated so as to remain in the grid voltage boundaries or to minimise the average voltage deviation of the network.

5.5 DVR REFERENCE VOLTAGE CALCULATION

The average voltage deviation of network can be minimised by DVR in an online manner by regulating the average network voltage to a pre-specified value, $V_{e}^{\text{ref}}$, which is typically 1 pu in order to benefit from increased efficiency of network as discussed in Section 1.1. The average voltage deviation can also be reduced with limited DVR power injection in order to only maintain bus voltages within the standard grid voltage limits. For these purposes, a reference voltage for DVR output must be calculated based on the obtained ELI and measurable parameters including $I_d$ and $V_s$. This shapes a feedforward control approach, since there is no feedback from bus voltages. Therefore, firstly, in (5.45), the Kirchhoff’s Voltage Law (KVL) for the line voltages is applied.

$$V_{e}^{\text{ref}} = V_s + V_{\text{DVR}} - Z_e I_d$$  \hspace{1cm} (5.45)

In order to obtain the value for the DVR reference voltage, equation (5.45) is rewritten as given in (5.46).

$$V_{e}^{\text{ref}} \angle \phi_e = V_s \angle 0 + V_{\text{DVR}} \angle \phi_{\text{DVR}} - Z_e I_d \angle \left( \phi_e + \phi_d \right)$$  \hspace{1cm} (5.46)
The reference angle is obtained from $V_{s1}$ as $\theta_{V_{s1}}$ using the already designed Phase-Locked Loop (PLL) in Chapter 3. Therefore, phase angle of this voltage is considered as zero. The active power consumption of the DVR is controlled to minimum possible so that the amount of active power required from the DC-link is minimised [137]. Thus, there is no need to use a rectifier for feeding the converter from grid, and a low rating source is used to compensate losses of the converter.

Therefore, in order to minimise the DVR active power consumption, the phase angle of the DVR voltage, $\phi_{DVR}$, which is in series with the line must be $90^\circ$ out of phase from line current as given in (5.47) to eliminates active power injection [113].

$$\phi_{DVR} = \phi_{d} + \pi/2$$

(5.47)

Figure 5.9 shows the phasor diagram of network parameters in presence of DVR compensation with the assumption that $V_e$ is equal to $V_{s1}$ in this case.

Voltage regulation with reactive power is most effective when bus power injections are pure reactive, and line impedances are pure inductive. This means that $I_d$ is $90^\circ$ lagged from $V_{s1}$, and consequently, $V_{DVR}$ is in phase with $V_{s1}$. Therefore, the voltage amplitude required from DVR to achieve a desired $V_e$ is minimised. Therefore, with more reactive bus injections and inductive line impedances, less voltage amplitude and reactive power from DVR is required. With pure active bus injections and resistive line impedances, $V_{DVR}$ is $90^\circ$ out of phase from $V_{s1}$, and therefore, the voltage amplitude required from DVR is maximised.

In order to calculate the required DVR voltage, (5.47) is replaced in (5.46), and the following equation is obtained.
\[
(V_{e_{ref}})^2 = V_{s1} + V_{rms_{DVR}}^2 \angle (\phi_{ld} + \pi/2) - Z_e I_d \angle (\phi_{Le} + \phi_{ld})^2
\]
which yields (5.49).

\[
(V_{e_{ref}})^2 = \left[ V_{s1} - V_{rms_{DVR}} \sin(\phi_{ld}) - Z_e I_d \cos(\phi_{Le} + \phi_{ld}) \right]^2
\]
\[
+ j \left[ V_{rms_{DVR}} \cos(\phi_{ld}) - Z_e I_d \sin(\phi_{Le} + \phi_{ld}) \right]^2
\]
Rearranging this equation in terms of DVR voltage magnitude leads to (5.50).

\[
\left( V_{rms_{DVR}} \right)^2 + b V_{rms_{DVR}} + c = 0
\]
where,

\[
b = -2 \left[ V_{s1} \sin(\phi_{ld}) + Z_e I_d \sin(\phi_{Le}) \right]
\]
\[
c = V_{s1}^2 - (V_{e_{ref}})^2 + Z_e^2 I_d^2 + 2 Z_e I_d V_{s1} \cos(\phi_{Le} + \phi_{ld})
\]
By solving (5.50), the reference voltage for DVR output is obtained as given in (5.53).

\[
V_{rms_{DVR}} = \left( -b \pm \sqrt{b^2 - 4c} \right) / 2
\]
\[
= V_{s1} \sin(\phi_{ld}) + Z_e I_d \sin(\phi_{Le})
\]
\[
\pm \sqrt{(V_{e_{ref}})^2 - \left[ V_{s1} \cos(\phi_{ld}) - Z_e I_d \cos(\phi_{Le}) \right]^2}
\]
with the condition in (5.54).

\[
|V_{e_{ref}}| \geq V_{s1} \cos(\phi_{ld}) - Z_e I_d \cos(\phi_{Le})
\]
The equation has two answers, but the answer with the smaller magnitude is used. Generally, distribution grids are inductive with negative \( \phi_{ld} \). This means that usually the positive sign gives the smaller magnitude.

### 5.5.1 Overvoltage and Under-voltage Limiting

If voltage deviations in the network are high, the grid voltage at downstream side of DVR, \( V_{s2} \), may need to cross either of the standard voltage limits so that the average voltage of the network is regulated to the pre-set value. In order to avoid the overvoltage and under-voltage, more computations are performed at each sampling.
step in order to find $V_{s2}$ based on the calculated DVR reference voltage to be compared with the voltage limits, as given in (5.55).

$$V_{s2} = V_{s1} + V_{DVR}^{rms} \angle \phi_{DVR} = \sqrt{V_{s1}^2 + (V_{DVR}^{rms})^2 + 2V_{s1}V_{DVR}^{rms} \cos(\phi_{DVR})}$$  \hspace{1cm} (5.55)$$

Thus, if $V_{s2}$ is going to cross the limits, DVR reference voltage is limited. The limited reference voltage is calculated by using (5.56) in order to limit the line voltage at the downstream side of DVR to $V_{s2}^{lim}$.

$$
\left(\frac{V_{s2}^{lim}}{V_{s1}}\right)^2 = \left(\frac{V_{s1}^{rms} \angle \phi_{DVR}}{V_{DVR}^{rms}}\right)^2
$$

The result is given in (5.57).

$$V_{DVR}^{rms,lim} = V_{s1} \sin(\phi_{d}) + \sqrt{\left[V_{s1} \sin(\phi_{d})\right]^2 + \left(V_{s2}^{lim}\right)^2 - V_{s1}^2}, \hspace{1cm} (5.57)$$

where $V_{s2}^{lim}$ is the higher limit of the grid voltage, if an overvoltage is going to happen, and it is the lower limit, if an under-voltage is going to happen. By using (5.53) and (5.57) in an online manner, the reference voltage magnitude for DVR is calculated. If this reference voltage with the phase angle in (5.47), as given in (5.58), is tracked by DVR output voltage, the average downstream network voltage will be regulated to the reference set point, $V_{e}^{ref}$.

$$V_{DVR}^{ref}(t) = \sqrt{2}V_{DVR}^{rms,lim} \cos(\theta_{s1} + \phi_{DVR})$$  \hspace{1cm} (5.58)$$

Nevertheless, the voltage regulation is also limited to the rated voltage of DVR. With limited rating, voltage deviation cannot be minimised, but it is still possible to keep bus voltages within boundaries. In addition, if the term to be root squared in (5.53) becomes negative, $V_{DVR}^{rms}$ is limited to $-b/2$. This is another limitation for voltage regulation which is variable and is imposed by network parameters.

**5.5.2 Compensation with Minimum DVR Voltage**

The calculated reference voltage for no active power injection does not minimise the magnitude of the compensation voltage of DVR. The phase angle of reference voltage can be defined so that the required compensation voltage is minimised. This approach has not been considered for simulation and optimisation, but its equations are obtained as follows. The minimum compensation voltage is
achieved when the DVR voltage is in phase with the series of upstream side line voltage, $V_{s1}$, and equivalent line voltage drop, $-Z_eI_d$, as illustrated in phasor diagram of Figure 5.10. Thus, for having a desired $V_e^{ref}$, an in phase component for DVR voltage is also obtained which shows that active power injection is required, and the DC source must be able to provide the active power.

Figure 5.10 Phasor diagram of the compensated network with DVR active power injection

$\phi_{DVR}$ in this case is calculated by (5.59).

$$\phi_{DVR} = \tan^{-1}\left[ \frac{Z_e I_d \sin(\phi_{Z_e} + \phi_{I_d})}{V_{s1} - Z_e I_d \cos(\phi_{Z_e} + \phi_{I_d})} \right]$$

(5.59)

The RMS DVR voltage magnitude is calculated using the KVL equation in (5.46) as follows.

$$V_{DVR}^{rms} = V_e^{ref} - \sqrt{Z_{s1}^2 + (Z_e I_d)^2 - 2V_{s1}Z_e I_d \cos(\phi_{Z_e} + \phi_{I_d})}$$

(5.60)

For overvoltage and under-voltage limiting of $V_{s2}$, this voltage is calculated at each sampling step by using (5.55). In case of voltage limit violation, the limited DVR reference voltage is enforced which is calculated using (5.56) and given in (5.61).

$$V_{DVR}^{lim.} = -V_{s1} \cos(\phi_{DVR}) + \sqrt{\left[V_{s1} \cos(\phi_{DVR})\right]^2 + \left(V_{s2}^{lim.}\right)^2 - V_{s1}^2}$$

(5.61)

Power rating of DC source must be more than the maximum output power of DVR.

### 5.6 REDUCTION OF HARMONIC VOLTAGE DISTORTION

Loads on the grid can be nonlinear, such as rectifiers, and therefore, branch currents can include some harmonic content. The main harmonics of the current are the 3rd, 5th, 7th and 9th harmonics. The harmonic voltage drops caused by these
currents degrade the voltage quality all over the network. In order to improve the voltage quality, DVR reference voltage needs to contain some compensating harmonic voltages as well as the fundamental frequency component. Harmonic compensation by a single DVR at one point cannot eliminate bus voltage distortions globally. However, elimination of harmonic content of the network equivalent voltage by proper harmonic voltage injection can reduce the average amount of distortion on all busses.

In order to calculate the compensating harmonic reference voltages for the converter, first, an ELI for the $h$-th harmonic order needs to be calculated as given in (5.62). The approach in Section 5.4 is used in which the harmonic load flow analysis gives the required information about the harmonic voltage deviation for calculation of ELI for each harmonic order as $Z_{e,h}$.

$$
Z_{e,h} = \sum_{j=1}^{L} \left\{ P\left(L_{j}\right) \cdot \frac{1}{M} \cdot \frac{BIBC_{b,1} \cdots BIBC_{b,N-1}}{B_{b,h}} \right\} \left( V_{b+1,h} - V_{h} \right) $$

Another approximation for the harmonic ELI is to consider the previously calculated ELI for the fundamental frequency voltage deviations. The reactive part of the ELI is multiplied by the harmonic order, $h$, as given in (5.63) in order to consider the variation of impedance caused by harmonic frequency.

$$
Z_{e,h} = R_{e} + jhX_{e} \quad \text{(5.63)}
$$

This estimation is closer to (5.62), if the harmonic power injection of buses are uniformly proportionate to their fundamental power injections. In addition, it can be used only when line capacitance admittances are not considerable up to the maximum harmonic frequency to be compensated. For calculation of harmonic reference voltages, equation (5.45) can be rewritten for each selected harmonic order as given in (5.64).

$$
V_{e,h}^{ref} = V_{s1,h} < 0 + \gamma_{DVR,h} - Z_{e,h}T_{d,h}, \quad \text{(5.64)}
$$

where $V_{e,h}$ is the network equivalent average harmonic voltage, and index $h$ shows the $h$-th order harmonic content. The phase angle of $V_{s1,h}$ is assumed to be zero, because the angle of the selected harmonic voltages are measured by the designed
PLL in Chapter 3 and used as the reference angles for the harmonic reference voltage generation.

For compensation of \( V_{e,h} \), the reference equivalent harmonic voltage deviation for each harmonic, \( V_{e,h}^{ref} \), must be set to zero. Moreover, minimising the power consumption of DVR is possible, if the phase angle of DVR reference voltage for each harmonic is 90° shifted from its corresponding line current harmonic as follows.

\[
\phi_{DVR,h} = \phi_{l,d,h} + \frac{\pi}{2}
\]  

With these assumptions, (5.66) is obtained.

\[
V_{s1,h} + V_{rms_{DVR,h}} = \left( \phi_{l,d,h} + \frac{\pi}{2} \right) - \left( \phi_{l,d,h} + \phi_{Z_{e,h}} \right) = 0
\]  

Solving this equation for required DVR harmonic voltage gives the following.

\[
V_{rms_{DVR,h}} = V_{s1,h} \sin \left( \phi_{l,d,h} \right) + Z_{e,h} I_{l,d,h} \sin \left( \phi_{Z_{e,h}} \right)
\]

\[
\pm \sqrt{-\left( V_{s1,h} \cos \left( \phi_{l,d,h} \right) - Z_{e,h} I_{l,d,h} \cos \left( \phi_{Z_{e,h}} \right) \right)^2} = 0
\]  

If DVR is placed at the secondary of the distribution transformer, and the harmonic content of \( V_{s1} \) is negligible, \( V_{s1,h} \) can be assumed as zero. From the remaining terms, the reference voltage for DVR can be simplified as follows.

\[
V_{rms_{DVR,h}} = Z_{e,h} I_{l,d,h} \left[ \sin \left( \phi_{l,d,h} \right) \pm \sqrt{-\cos^2 \left( \phi_{Z_{e,h}} \right)} \right]
\]  

The equations (5.67) and (5.68) shows that with no active power injection from DVR, the harmonic compensation is always limited to the real part of the reference voltage. With the limited referenced voltage, amplitude of \( V_{e,h} \) can be minimised as given in (5.69) by replacing the real part of (5.67) in (5.64).

\[
V_{e,h} = \left[ V_{s1,h} \cos \left( \phi_{l,d,h} \right) - Z_{e,h} I_{l,d,h} \cos \left( \phi_{Z_{e,h}} \right) \right]
\]  

The equation shows that generally, harmonics of the equivalent voltage cannot be eliminated. If \( V_{s1,h} \) is considered as negligible, complete elimination is possible only when \( \phi_{Z_{e,h}} = \pi/2 \), i.e. an inductive line impedance. In an LV grid, with a ratio of about one for \( R_e \) to \( X_e \), line impedance will be closer to inductive impedance only for
high order harmonics. With this assumption, the value of \( \cos(\phi_{Z_e,h}) \) for the third, fifth and seventh harmonics are about 0.32, 0.20 and 0.14, respectively.

However, if active power injection at harmonic frequencies is desired, the reference voltage can be calculated as given in (5.70). Harmonics of \( V_s \) are also included as a general case, when DVR is located in a place where the harmonics are not negligible.

\[
V_{rms_{DVR,h}} \angle \phi_{DVR,h} = Z_{e,h} I_{d,h} \angle (\phi_{Z_e,h} + \phi_{d,h}) - V_{s1,h}
\]

\[
= \sqrt{Z_{e,h}^2 I_{d,h}^2 + V_{s1,h}^2 - 2Z_{e,h} I_{d,h} V_{s1,h} \cos(\phi_{Z_e,h} + \phi_{d,h})}
\]

\[
\tan^{-1}\left( \frac{Z_{e,h} I_{d,h} \sin(\phi_{Z_e,h} + \phi_{d,h})}{Z_{e,h} I_{d,h} \cos(\phi_{Z_e,h} + \phi_{d,h}) - V_{s1,h}} \right)
\]

This equation can be simplified to (5.71) when harmonic content of \( V_s \) is negligible.

\[
V_{rms_{DVR,h}} \angle \phi_{DVR,h} = Z_{e,h} I_{d,h} \angle (\phi_{Z_e,h} + \phi_{d,h})
\]

Thus, the reference voltage for DVR is calculated as follows.

\[
v_{ref}^{C_f}(t) = \sqrt{2} V_{rms,lim_{DVR}} \cos(\theta_{V_s1} + \phi_{DVR}) + \sqrt{2} \sum_{h=3,5,7} V_{rms_{DVR,h}} \cos(\theta_{V_{s1,h}} + \phi_{DVR,h}).
\]

5.7 MEASUREMENT OF LINE CURRENT HARMONICS

Magnitude and phase angle of line current harmonics, \( I_{d,h} \) and \( \phi_{d,h} \), are measured by single-phase SRF transformation of the line current signal in an open loop configuration. The \( \alpha'\beta' \) components for each selected harmonic are generated by a Second Order Generalised Integrator-Quadrature Signal Generator (SOGI-QSG). The centre frequency of each SOGI is equal to the corresponding harmonic frequency. The fundamental frequency already measured by PLL from \( V_s \) is multiplied by the harmonic order to find the centre frequency for each harmonic stage. The reference angle for SRF transformation is also acquired from the measured angle of \( V_s \) for each selected harmonic, \( \theta_{V_{s1,h}} \), by the already designed PLL.

It was shown in equation (3.3) that the obtained \( dq \) components contain the even harmonics generated by the odd harmonics of the line current. A MAF with proper
window length can eliminate this harmonic content. Finally, the magnitude and phase angles are calculated from the averaged \(dq\) components as follows.

\[
I_{d,h} = \sqrt{\left(\frac{i_{d,h}}{2}\right)^2 + \left(\frac{i_{q,h}}{2}\right)^2}, \quad (5.73)
\]

\[
\phi_{i_{d,h}} = \arctan2\left(\frac{i_{q,h}}{i_{d,h}}\right), \quad (5.74)
\]

where ‘\(\arctan2\)’ function return the appropriate quadrant of the computed angle.

Figure 5.11 shows the block diagram for line current measurement.

In addition, if \(I_d\) is too small, a zero average voltage drop is estimated for the downstream network. However, DVR may still need to inject a non-zero voltage for regulation of \(V_{es}\) because the voltage at its upstream side, \(V_{s1}\), may be not equal to the desired average voltage for downstream network, \(V_{e ref}\). Small \(I_d\) cannot be measured accurately, and equation (5.74) does not give a certain value for \(\phi_{i_d}\). This results in calculation of an uncertain value for DVR reference voltage. Therefore, \(\phi_{i_d}\) is considered as a constant value, like \(-\pi/2\), when calculated \(I_d\) is smaller than a threshold value.
The SOGI filter can provide some filtering which is required for proper implementation of the algorithm. The transients of the line current caused by load and PV connections and disconnections can adversely affect the transient calculated value of DVR reference voltage. This may lead to high overshoots in the transient response or may even cause instability of the network. In addition to this, the calculated reference voltage is also filtered at the output by using a Low Pass Filter (LPF). This extra filtering is necessary, because the limited output voltage and mathematical conditions, such as (5.54), will introduce nonlinearity in the control loop. LPF limits the bandwidth of reference generation loop which filters the nonlinear response and smooths the loop operation. The damping coefficient of SOGI, \( k \), and the LPF cut-off frequency are set to appropriate values so as to have some filtering as well as a desirable response time. With the value of \( k \) equal to 1.41 and the LPF cut-off frequency of 10 rad/s, a good and stable response was achieved. Figure 5.12 shows the block diagram for reference voltage calculation.

![Block diagram of DVR reference voltage generation](image)

**5.8 VOLTAGE REGULATION WITH SHUNT COMPENSATION**

D-STATCOM is a VSC which is placed in parallel to the network at a bus to achieve various objectives by injecting or absorbing reactive power, as depicted in Figure 5.13. It can be used for voltage regulation and compensation, power factor correction and current harmonic elimination. The load flow analysis with presence of D-STATCOM can be performed by manipulating the typical load flow analysis. The D-STATCOM current injection at its bus is added to the bus current injection. The current injection matrix, \( I \), which was calculated by (5.6) must be modified as given in (5.75).
In order to minimise the active power consumption of converter, the output current phase has to be lagged from the grid voltage phase at the converter feeder, $V_{s2}$, by 90° as follows.

$$\phi_{i_{\text{STATCOM}}} = \phi_{s2} - \frac{\pi}{2}$$

(5.77)

The load flow analysis is used in the optimisation process for D-STATCOM rating and placement. A similar optimisation procedure to that of DVR is performed with the new decision variable, $I_{\text{STATCOM}}$, which is included in the particle vector, as illustrated in Figure 5.14.

In order to compare the required reactive power rating of the converter for the two types of series and shunt compensation, the reactive output power for both the cases in a same application are compared. The schematics for two simple cases are depicted in Figure 5.15 and Figure 5.16 where the converters are located at the secondary side of the distribution transformer.
The results for DVR and D-STATCOM output reactive power are given in (5.78) and (5.79), respectively.

\[ Q_{DVR} = V_{DVR} I_d = Q_{line} + Q_t = Q_{line} + \frac{V_{s1} (V_{s1} - V_1)}{X_t}, \quad (5.78) \]

\[ Q_{D-STATCOM} = V_{s2} I_{STATCOM} = Q_{line} + Q_t = Q_{line} + \frac{V_{s2} (V_{s2} - V_1)}{X_t}, \quad (5.79) \]

where the equation for reactive power transfer of an inductive feeder in (5.80) is used. \( V_1 \) and \( V_2 \) are the RMS voltage magnitudes at the two sides of feeder.

\[ Q_{feeder} = \frac{V_1 (V_1 - V_2)}{X_{feeder}} \quad (5.80) \]

Equation (5.79) show that output reactive power of D-STATCOM is dependent on the grid voltage at the converter feeder, \( V_{s2} \). This voltage must be varied in the allowable range of the grid voltage, based on the amount of loads in order to regulate \( V_e \). This high range of voltage variation as well as the small value of \( X_t \) implies a high reactive power requirement from D-STATCOM to feed the upstream network which may need a high amount of reactive power. This makes the power injection of the shunt compensation be highly dependent on the upstream network parameters. On the contrary, DVR output power in (5.78) is dependent on the voltage at the transformer side, \( V_{s1} \). Unlike \( V_{s2} \), the variations of this voltage during regulation are very small. Therefore, the absorbed or injected reactive power by DVR is much less sensitive to the upstream network.
Therefore, for the same application, DVR is more effective than D-STATSOM due to its lower power rating requirement. DVR as a series connected device is more suitable for limiting fault currents as well. Additionally, DVR can be used for voltage harmonic compensation and voltage transient reduction [138]. It is more effective for voltage harmonic compensation at the load than D-STATCOM, because shunt compensator can circulate load harmonic currents, but it is not as effective in compensating voltage harmonics.

Nonetheless, the compensation by DVR brings up new protection challenges because of the series connection and the high current flow through the device, which are main drawbacks of using DVR in distribution networks, as discussed in Section 4.2. In addition, the limited output admittance of the series connected device increases the harmonic voltage drop in the line, and therefore, the converter output filter or control algorithm needs refining in order to reduce or eliminate the harmonic voltage drop. Moreover, the series connected device cannot mitigate voltage interruptions unlike a shunt compensator with enough active power rating [139].

5.9 IMPLICATIONS OF EXTENDING TO THREE-PHASE AND RING NETWORKS

The proposed algorithms for single-phase regulation can be extended for three-phase applications. The algorithms can, therefore, be developed in order to decrease the amount of unbalance in three-phase networks.

If major loads of the network are single-phase, minor unbalances can be neglected. However, three-phase loads may encounter serious problems in unbalanced conditions [140]. Therefore, one single-phase DVR at an optimum location for each phase of the three-phase network can minimise average voltage deviation in the three-phase system which improves voltage unbalances. The algorithm can also be further improved to reduce the phase unbalances by minimising the phase unbalance of the equivalent voltage. However, this may require active power injection by DVRs because of a defined set-point for phase.

As another approach, a three-phase topology can be utilised such that one three-phase DVR improves the voltage regulation and unbalance as well as phase unbalance. The optimisation algorithm must be modified in order to include the entire three-phase network in finding an optimal location for the three-phase DVR.
such that the desired optimisation objective is achieved for the whole system. For three-phase implementation, an appropriate three-phase reference voltage including positive, negative and zero sequence voltage references needs to be generated by the regulation algorithm and tracked by the three-phase converter output with a proper tracking control algorithm.

An advantage of three-phase inverters is the minimised AC current in the DC-link unlike single-phase inverters in which a second order harmonic current flows through the DC-link. In three-phase inverters with balanced and linear load, there is no AC current flow through the DC-link. Therefore, if no active power or harmonic injection by DVR is required, DC source can be removed, and voltage of the DC-link capacitor can be maintained at a desired value by feeding the DVR via its output with active power required for compensation of its losses from the grid. This is possible by a control loop to adjust the phase angle of the output voltage in order to have a negative active power flow. Nonetheless, the unbalanced and harmonic currents may introduce some harmonic ripples into the DC-link capacitor voltage.

In addition to control algorithms, SRF-PLL needs to be extended for three-phase applications to be able to measure positive, negative and zero sequence components of the grid voltage for generating a proper compensating voltages for the entire sequences, and also synchronise the converter with these sequences. The unbalanced signals introduce a second order harmonic component into the PLL control loop which must be eliminated by a proper algorithm [141] such as using a MAF.

It is also worth noting that the proposed regulation and voltage quality improvement algorithm is designed for radial networks, because in this case, the estimation of average voltage deviation can be obtained using locally measured parameters at DVR. However, in ring networks, estimating the average voltage deviation may require communication links to collect some data from other parts of the network in addition to the locally measured data. Nonetheless, the proposed communication-less algorithm can be applied to radial branches originating from any ring network.

5.10 OPTIMISATION STUDIES

In this section, the optimisation for the DVR location in the sample 6-bus network in Figure 5.5, distribution transformer tap setting and DVR sizing is performed, with hypothetical clustered load and generation levels using MATLAB
software. The algorithms can be performed on larger networks as well, when clustering is applied to all buses, and clustered load levels are obtained.

Buses are assumed to have similar constant impedance, constant current and constant power demand shares of 50%, 0% and 50%, respectively as well as similar power factor of 0.85 which are typical values for residential grids. The nominal clustered demand and generation power rating of buses is given in Table 5.2. The duration of clustered load levels are also provided in the table. The base per unit power, $S_{\text{base}}$, is considered as 5 kVA, and the base voltage of the single-phase grid, $V_{\text{base}}$, is considered as the nominal 239.6 V. Hence, $I_{\text{base}}$ is equal to 20.9 A, and $Z_{\text{base}}$ is 11.5 $\Omega$. The standard grid voltage limits are considered as $1\pm6\%$ pu for 240 V/415 V line voltage, and therefore, $V_{\text{lo}}$ is 0.94 pu and $V_{\text{hi}}$ is 1.06 pu.

**Table 5.2 Network parameters in different load levels**

<table>
<thead>
<tr>
<th>Bus Number</th>
<th>Load Level 1 (pu)</th>
<th>Load Level 2 (pu)</th>
<th>Load Level 3 (pu)</th>
<th>Load Level 4 (pu)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_{\text{di}}^{\text{nom}}$</td>
<td>$Q_{\text{di}}^{\text{nom}}$</td>
<td>$P_{\text{gi}}^{\text{nom}}$</td>
<td>$Q_{\text{gi}}^{\text{nom}}$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0.80</td>
<td>0.50</td>
<td>0.10</td>
<td>0.60</td>
</tr>
<tr>
<td>3</td>
<td>1.10</td>
<td>0.68</td>
<td>0.20</td>
<td>0.80</td>
</tr>
<tr>
<td>4</td>
<td>1.20</td>
<td>0.74</td>
<td>0.10</td>
<td>1.00</td>
</tr>
<tr>
<td>5</td>
<td>1.20</td>
<td>0.74</td>
<td>0.10</td>
<td>1.20</td>
</tr>
<tr>
<td>6</td>
<td>1.30</td>
<td>0.81</td>
<td>0.10</td>
<td>1.35</td>
</tr>
<tr>
<td>$P(L_j)$</td>
<td>15%</td>
<td>25%</td>
<td>35%</td>
<td>25%</td>
</tr>
</tbody>
</table>

Five branches of the network are assumed to have similar impedance per kilometre with different lengths as given in Table 5.3.

**Table 5.3 Network branch parameters**

<table>
<thead>
<tr>
<th>Branch Number</th>
<th>$R$ ($\Omega$/km)</th>
<th>$X$ ($\Omega$/km)</th>
<th>Length (m)</th>
<th>Impedance (pu)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.786</td>
<td>0.745</td>
<td>80</td>
<td>$(5.477+5.191)\times10^{-3}$</td>
</tr>
<tr>
<td>2</td>
<td>0.786</td>
<td>0.745</td>
<td>60</td>
<td>$(4.107+3.893)\times10^{-3}$</td>
</tr>
<tr>
<td>3</td>
<td>0.786</td>
<td>0.745</td>
<td>130</td>
<td>$(8.899+8.435)\times10^{-3}$</td>
</tr>
<tr>
<td>4</td>
<td>0.786</td>
<td>0.745</td>
<td>90</td>
<td>$(6.161+5.840)\times10^{-3}$</td>
</tr>
<tr>
<td>5</td>
<td>0.786</td>
<td>0.745</td>
<td>70</td>
<td>$(4.792+4.542)\times10^{-3}$</td>
</tr>
</tbody>
</table>

The hybrid constriction coefficient PSO-GA introduced in Section 2.3.1 with parameters listed in Table 5.4 is used for optimisation. A probability of 50% is
considered for crossover among particles, and thus, about half of particles are selected for crossover in every iteration step. Decision variable constraints for all optimisation studies are already given in Table 5.1.

<table>
<thead>
<tr>
<th>Table 5.4 PSO-GA parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Iterations</td>
</tr>
<tr>
<td>Number of Runs</td>
</tr>
<tr>
<td>Particle Population</td>
</tr>
<tr>
<td>( \varphi_{\text{max}} )</td>
</tr>
<tr>
<td>( \varphi_1=\varphi_2 )</td>
</tr>
<tr>
<td>( k )</td>
</tr>
<tr>
<td>Crossover Probability</td>
</tr>
<tr>
<td>Maximum Convergency Error</td>
</tr>
</tbody>
</table>

Figure 5.17 illustrates the load flow analysis results without DVR and with different tap settings for distribution transformer. It is observed that fixed tap setting cannot provide a good regulation in all the load levels, and some buses may suffer from both the overvoltage and under-voltage or either of them in different load levels. Thus, implementing a voltage regulation scheme is necessary for this network.

![Figure 5.17 Bus voltage magnitudes in different load levels and with different tap settings, 0%, +2.5% and +5%](image-url)

---

168 Chapter 5: Grid Voltage Quality Improvement Using DVR
Table 5.5 also includes network parameters including average bus voltage deviation and network power loss for different tap settings.

<table>
<thead>
<tr>
<th>Tap Setting (%)</th>
<th>5</th>
<th>2.5</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V_e$ (%) pu</td>
<td>4.133</td>
<td>3.495</td>
<td>4.267</td>
</tr>
<tr>
<td>Average $P_{loss}$ (pu)</td>
<td>0.1509</td>
<td>0.1530</td>
<td>0.1555</td>
</tr>
</tbody>
</table>

5.10.1 Case 1: Optimisation for Voltage Deviation Minimisation

The optimisation is performed for different definitions of objective function. First, it is performed for finding the optimised decision variables for the objective of best regulation using the objective function in (5.32). Optimisation results for 100 executions of the algorithm as well as some network parameters including minimised average bus voltage deviation and network power loss are given in Table 5.6. The results show that in spite of the implemented GA crossover for escaping from suboptimal solutions, optimisation can still find some suboptimal solutions with lower probability densities. Nonetheless, because they are very close to the optimal solution in the value of the objective function, the Coefficient of Variation (CV) is small. The number of iterations also shows that the optimisation process is converged with limited iterations. To select a proper solution, the other calculated design parameters provided in the table which have not been included in the objective function can be considered. Among all solutions, the one with the least power rating for DVR and with the least average voltage deviation is selected in which the optimal tap setting is 2.5% and optimal DVR location is at bus number 3 in branch number 2.

<table>
<thead>
<tr>
<th>Tap Setting (%)</th>
<th>5</th>
<th>2.5</th>
<th>0</th>
<th>-2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Number</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>$\Delta V_e$ (%) pu</td>
<td>1.307</td>
<td>1.270</td>
<td>1.294</td>
<td>1.301</td>
</tr>
<tr>
<td>$S_{DVR}$ (pu)</td>
<td>0.9118</td>
<td>0.6929</td>
<td>0.9733</td>
<td>0.9929</td>
</tr>
<tr>
<td>Average $P_{loss}$ (pu)</td>
<td>0.1605</td>
<td>0.1596</td>
<td>0.1599</td>
<td>0.1602</td>
</tr>
<tr>
<td>No. of Iterations</td>
<td>78</td>
<td>79</td>
<td>78</td>
<td>75</td>
</tr>
<tr>
<td>Probability Density</td>
<td>12%</td>
<td>34%</td>
<td>25%</td>
<td>13%</td>
</tr>
<tr>
<td>Objective Function</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 5.18 shows the decision variable values during the optimisation process as particle movement to converge to this optimum solution. Figure 5.19 illustrates the load flow analysis results before and after placing the DVR in the network.
Figure 5.18 Decision variables values as particle movement during the optimisation process

Figure 5.19 Bus voltage magnitudes in different load levels without DVR (blue), and with optimised voltage and location of DVR for voltage deviation minimisation (red and green)
It can be observed that DVR can provide a good regulation in all the load levels such that over and under-voltages are avoided. The regulation increases the efficiency of electric motor loads and reduces network losses as discussed in Section 1.1. In a typical grid, PV stops injecting as soon as an overvoltage occurs at the bus. Therefore, the power injection will be stopped at some of these buses such that overvoltage is avoided all over the network as simulated in Section 5.11. This clustered load level has duration of 25% during a year, and loss of generation for this period greatly reduces the effectiveness of PV penetration in the network. However, after placement of DVR, all the voltages have been regulated to remain close to 1 pu in all the clustered load levels, and therefore, the loss of PV energy is avoided.

5.10.2 Case 2: Optimisation for Power Loss and DVR Rating Minimisation

Optimisation is also performed for minimising the average power loss and DVR rating using objective functions in (5.35) and (5.37), respectively. As indicated in Table 5.7 for 100 runs, optimisation for network power loss minimisation also finds some suboptimal solutions with low probability densities but close to the global optimal solutions. The solution with 2.5% tap setting and DVR location at bus number 4 suggests the least rating for DVR.

<table>
<thead>
<tr>
<th>Tap Setting (%)</th>
<th>5</th>
<th>2.5</th>
<th>0</th>
<th>-2.5</th>
<th>Objective Function</th>
<th>Bus Number</th>
<th>Average $P_{loss}$</th>
<th>$S_{DVR}$ (pu)</th>
<th>$\Delta V_e$ (%) pu</th>
<th>No. of Iterations</th>
<th>Probability Density</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>Mean</td>
<td>2</td>
<td>0.1541</td>
<td>0.4100</td>
<td>2.970</td>
<td>172</td>
<td>9%</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1536</td>
<td>1541</td>
<td>1541</td>
<td>Standard Deviation</td>
<td>2</td>
<td>0.1538</td>
<td>0.5583</td>
<td>3.083</td>
<td>174</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>-2.5</td>
<td>0.6427</td>
<td>0.9524</td>
<td>2.970</td>
<td>Coefficient of Variation</td>
<td>4</td>
<td>0.1541</td>
<td>9%</td>
<td>162</td>
<td>152</td>
<td>9%</td>
</tr>
<tr>
<td></td>
<td>10%</td>
<td>2.281×10^{-4}</td>
<td>0.148%</td>
<td>2.970</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Optimisation for DVR rating finds only one optimal solution suggesting a much smaller DVR compared to the two previous optimisation cases, as given in Table 5.8. The number of iterations is increased, but the optimisation process can converge to the optimal solution. In this case, bus voltages can vary in the allowable range of grid voltage, and no constraints are enforced for average voltage deviation. The only constraint is the added over and under-voltage penalty term to the objective function, and therefore, DVR rating is so much that it can only maintain bus voltages in the allowable region in all the load levels, as illustrated in Figure 5.20 and Figure 5.21.
Figure 5.20 Decision variables values as particle movement during the optimisation process

Figure 5.21 Bus voltage magnitudes in different load levels for DVR rating minimisation, without DVR (blue), and with optimised voltage and location for DVR (red and green)

Chapter 5: Grid Voltage Quality Improvement Using DVR
Generally, keeping bus voltages within this range is the target of regulation that can be achieved by a smaller DVR.

Table 5.8 Optimisation results for DVR rating minimisation

<table>
<thead>
<tr>
<th>Tap Setting (%)</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Number</td>
<td>4</td>
</tr>
<tr>
<td>$S_{DVR}$ (pu)</td>
<td>0.1576</td>
</tr>
<tr>
<td>$\Delta V_e$ (% pu)</td>
<td>2.718</td>
</tr>
<tr>
<td>Average $P_{loss}$</td>
<td>0.1546</td>
</tr>
<tr>
<td>No. of Iterations</td>
<td>254</td>
</tr>
<tr>
<td>Probability Density</td>
<td>100%</td>
</tr>
</tbody>
</table>

5.10.3 Case 3: Optimisation for Multi-Objective Cost Function

Weighting coefficients of the multi-objective cost function in (5.40) can be selected such that the cost function reflects the real cost of implementation and electricity loss in order to minimise the total investment cost using objective function in (5.41). However, a balance between different targets can also be achieved by manipulating the weightings based on the obtained results in Table 5.6 and Table 5.7 and by trial and error. Based on the obtained results, in order to have similar importance for loss (about 0.15 pu) and deviation (about 1.3% pu), the loss weighting is chosen as 8.7 times the deviation weighing. The weighting of rating can be selected based on the trial and error, i.e. by executing the optimisation for different values of weighting such that a desired balance is achieved. Bus voltage magnitudes with weighted optimisation are plotted in Figure 5.22, and the summarised optimisation results in Table 5.9 shows that there is a global optimal solution with high probability density, and a balance between objectives has been achieved.

Table 5.9 Optimisation results for weighted objective function

<table>
<thead>
<tr>
<th>Weightings</th>
<th>$w_D = 1$, $w_L = 8.7$, $w_R = 2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tap Setting (%)</td>
<td>2.5</td>
</tr>
<tr>
<td>Bus Number</td>
<td>3</td>
</tr>
<tr>
<td>$\Delta V_e$ % pu</td>
<td>1.499</td>
</tr>
<tr>
<td>$S_{DVR}$ (pu)</td>
<td>0.41</td>
</tr>
<tr>
<td>Average $P_{loss}$ (pu)</td>
<td>0.1585</td>
</tr>
<tr>
<td>No. of Iterations</td>
<td>96</td>
</tr>
<tr>
<td>Probability Density</td>
<td>82%</td>
</tr>
<tr>
<td>Objective Function</td>
<td></td>
</tr>
<tr>
<td>Mean</td>
<td>3.8050</td>
</tr>
<tr>
<td>Standard Deviation</td>
<td>0.2567</td>
</tr>
<tr>
<td>Coefficient of Variation</td>
<td>6.7455%</td>
</tr>
</tbody>
</table>
The optimisation for D-STATCOM rating and placement is also performed in order to compare the usage of DVR and D-STATCOM in a similar network. D-STATCOM output current is limited to ±1 pu for optimisation so as to have similar power rating limit to that of designed DVR, and the two other variables are limited the same as before. The optimisation results for objective function in (5.32), (5.35) and (5.37) are provided in Table 5.10. The optimum tap setting and location for all the objectives are 2.5% and bus number 5, respectively. Compared to DVR optimisation cases, there are no suboptimal solutions for any of the performed optimisations which indicate zero standard deviations.

Comparing optimisation results with the ones in Table 5.6, Table 5.7 and Table 5.8 shows that shunt compensation with similar power rating is less effective than series compensation in reducing voltage deviations as previously discussed in Section 5.8. However, as optimisation results for power loss minimisation shows, it could be more effective in reducing network power losses. The load flow analysis with the results of optimisation for voltage deviation minimisation are plotted in Figure 5.23.
which shows that some bus voltages have crossed the standard grid voltage limits, and D-STATCOM with the limited output current of ±1 pu cannot maintain bus voltages in the allowable range in all the load levels.

Table 5.10 Optimisation results for different objective functions for D-STATCOM

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Voltage Deviation Optimisation</th>
<th>Power Loss Optimisation</th>
<th>STATCOM Rating Optimisation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tap Setting (%)</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Bus Number</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>ΔVe (% pu)</td>
<td>2.574</td>
<td>2.916</td>
<td>3.210</td>
</tr>
<tr>
<td>SSTATCOM (pu)</td>
<td>1.047</td>
<td>0.9727</td>
<td>0.4561</td>
</tr>
<tr>
<td>Average Ploss</td>
<td>0.1472</td>
<td>0.1341</td>
<td>0.1463</td>
</tr>
<tr>
<td>No. of Iterations</td>
<td>82</td>
<td>169</td>
<td>225</td>
</tr>
<tr>
<td>Probability Density</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
</tr>
</tbody>
</table>

Figure 5.23 Bus voltage magnitudes in different load levels for deviation minimisation, without D-STATCOM (blue), and with optimised current and location for D-STATCOM (red and green)

For achieving a similar voltage deviation as the one obtained with DVR in Table 5.6 (1.270 pu deviation with 0.6929 pu DVR rating), the output current limit was further increased to 2.807 pu. The optimisation for minimum average deviation results in 2.814 pu rating for D-STATCOM located at bus number 5 and with tap setting of 2.5%. Therefore, the rating must be 4.06 times that of DVR in order to have a similar
voltage regulation. However, DVR drawbacks including cost of protection devices
and high current flow through the series connected device may make it less
beneficiary in terms of investment cost, as discussed in Section 5.8.

Table 5.11 Optimisation results for D-STATCOM rating minimisation

<table>
<thead>
<tr>
<th>Tap Setting (%)</th>
<th>5</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Number</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>$S_{D-STATCOM}$ (pu)</td>
<td>1.637</td>
<td>1.366</td>
</tr>
<tr>
<td>$\Delta V_e$ (% pu)</td>
<td>2.963</td>
<td>2.890</td>
</tr>
<tr>
<td>Average $P_{loss}$ (pu)</td>
<td>0.1708</td>
<td>0.1407</td>
</tr>
<tr>
<td>No. of Iterations</td>
<td>279</td>
<td>252</td>
</tr>
<tr>
<td>Probability Density</td>
<td>36%</td>
<td>64%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Objective Function</th>
<th>Mean</th>
<th>1.437</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Standard Deviation</td>
<td>0.1782</td>
</tr>
<tr>
<td></td>
<td>Coefficient of Variation</td>
<td>12.1%</td>
</tr>
</tbody>
</table>

Figure 5.24 Bus voltage magnitudes in different load levels for power rating minimisation with
increased output current limit, without D-STATCOM (blue), and with optimised current and location
for D-STATCOM (red and green)

In order to maintain bus voltages within the standard limits, the optimisation is
performed for D-STATCOM power rating minimisation and with the previously
increased output current limit. As summarised in Table 5.11, global optimum
solution suggest 1.366 pu power rating with placement at bus number 5 and 2.5% tap
setting. As plotted in Figure 5.24, voltage limit violations are resolved. Comparison
with DVR case in Table 5.8 shows that the rating is 8.7 times the DVR rating.
5.11 SIMULATION STUDIES

After finding the optimal location and tap setting, in order to investigate the transient operation of DVR and validate the designed converter control and online voltage regulation algorithms, the 6-bus network in Figure 5.5 with parameters listed in Table 5.2 and Table 5.3 was modelled in PSCAD-EMTDC. Constant power injection, which includes the constant power load and generation, was modelled by a voltage source controlled in an open loop configuration. It injects the desired power to the network via a feeder as depicted in Figure 5.25.

\[ S_{\text{ref}} = \alpha^{\text{PQ}} S_{\text{nom}} + S_{\text{g}} = P_{\text{ref}} + jQ_{\text{ref}} = V_2^2 - V_2 V_1^* = Z_f^* \]

\[ \phi_1 = \arctan \left( \frac{R_f Q_{\text{ref}} - X_f P_{\text{ref}}}{V_2^2 - R_f P_{\text{ref}} - X_f Q_{\text{ref}}} \right), \]

\[ V_1 = \frac{R_f Q_{\text{ref}} - X_f P_{\text{ref}}}{V_2 \sin(\phi_1)}, \]

\[ v_1(t) = \sqrt{2} V_1 \cos(\phi_2 + \phi_1), \]

where, \( \phi_1 \) and \( V_1 \) are the phase angle and RMS magnitude of the reference voltage, and \( R_f \) and \( X_f \) are the resistance and inductance of the bus feeder. Calculation of resistance and reactance of constant impedance loads can be performed as follows.
\[ Z_{\text{load}} = R_{\text{load}} + jX_{\text{load}} = (V_{\text{nom}})^2 \]

\[ = \frac{100}{0.01} \]

(5.85)

The ELI is calculated by using (5.44) to obtain \( Z_e = (3.3594 + j 3.004) \times 10^{-3} \text{ pu} \).

Before presenting the simulation results, bus voltage magnitudes, \( V_{2\ldots6} \), and network bus voltage deviation, \( \Delta V_e \), for all the load levels are simulated and plotted in Figure 5.26 in order to confirm the validity of the model and observe the voltage rise and drop issues. Then, different simulation cases are considered as follows.

**Figure 5.26** (a) bus voltage magnitudes and (b) deviation in load levels 2, 1, 3 and 4, respectively

### 5.11.1 Case 1: PV Overvoltage Protection Performance

In this case, the simulation is performed to evaluate the network operation with PV overvoltage protection. If an overvoltage of more than 6\% is measured locally on
a bus for a specified amount of time, the PV inverter is tripped and disconnected from the bus. It is assumed that overvoltage must be seen for three main cycles (60 ms) in order for the disconnection to be triggered. For this purpose, a delay timer is started for overvoltage protection reaction, and if the overvoltage is removed from the bus during the delay, the timer is reset. In the fourth load level, high PV generation causes overvoltage in some buses. Figure 5.27 shows bus voltages when injection in this load level is started. After about three cycles, the buses which have sensed the overvoltage earlier, including buses number 4 and 5, stop injecting. This drops the voltages at other buses such that they may not trip.

![Figure 5.27 (a) bus voltages, and (b) output power of PV inverter with overvoltage protection](image)

This control strategy is the currently applied method for avoiding overvoltage in the LV grids with PV generation. It can be observed that the application of this traditional control strategy can cause the loss of a huge amount of energy on a large
scale, and therefore, it can be avoided by voltage regulation using DVR, as illustrated in later simulation cases.

5.11.2 Case 2: Active Power Curtailment Performance

In this case the active power curtailment method presented in [98] is simulated. This method uses the droop control in order to make the injected power by inverter a function of bus voltage, $V$, as given in (5.86).

$$P_{inv} = P_{MPPT} - m(V - V_{th}), \quad V > V_{th}, \quad P_{inv} > 0,$$

(5.86)

where the PV inverter is controlled with the maximum power point tracking (MPPT) algorithm, and therefore, $P_{MPPT}$ is the maximum available PV power which varies based on the solar irradiance, $m$ is the slope factor (kW/V), and $V_{th}$ is the threshold voltage for activating the output power reduction by droop function. The slope factor and threshold voltage are selected based on the value of higher voltage limit of the grid, $V_{hi}$, and maximum power of inverter in order to coordinate PV inverters for sharing the active power curtailment such that all bus voltages remain in the allowable range. Therefore, $m$ is calculated as follows [98].

$$m = \frac{P_{MPPT}}{V_{hi} - V_{th}},$$

(5.87)

The value of $V_{th}$ is chosen to be 1.043 pu [98], and $V_{hi}$ is 1.06 pu. The active power is curtailed linearly based on the local bus voltage, $V$, if this voltage is greater than $V_{th}$. The power reduction continues until $V$ reaches $V_{hi}$, where the output power is reduced to zero.

Figure 5.28 (a) shows bus voltages when inverters start injecting in the fourth load level and the active power curtailment is active. This approach maintains bus voltages within the standard range and prevents the overvoltage protection from triggering. The output active power of inverters, $P_{inv}$, is plotted in Figure 5.28 (b). This control strategy causes the loss of renewable energy which is not desirable for future smart grids. As given in Table 5.12, it has reduced the total generated power by about 17.4%. If a higher distribution transformer tap is set, the reduction in generated power will be higher. It can also be observed that droop curtailment has the benefit of power reduction sharing among the inverters whose bus voltage is greater than $V_{th}$. 

180 Chapter 5: Grid Voltage Quality Improvement Using DVR
Table 5.12 Nominal and curtailed active power generation at buses

<table>
<thead>
<tr>
<th>Bus Number</th>
<th>$P_{\text{nom}}^{\text{gi}}$</th>
<th>$P_{\text{inv}}^{\text{iP}}$</th>
<th>$V_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.20</td>
<td>1.2</td>
<td>1.035</td>
</tr>
<tr>
<td>3</td>
<td>1.35</td>
<td>1.35</td>
<td>1.039</td>
</tr>
<tr>
<td>4</td>
<td>1.40</td>
<td>0.991</td>
<td>1.048</td>
</tr>
<tr>
<td>5</td>
<td>1.50</td>
<td>0.872</td>
<td>1.050</td>
</tr>
<tr>
<td>6</td>
<td>0.50</td>
<td>0.5</td>
<td>1.036</td>
</tr>
<tr>
<td><strong>Total Power (pu)</strong></td>
<td><strong>5.95</strong></td>
<td><strong>4.913</strong></td>
<td></td>
</tr>
</tbody>
</table>

Figure 5.28 (a) Bus voltage magnitudes, and (b) PV inverter output power with active power curtailment

5.11.3 Case 3: Online Voltage Regulation Algorithm Performance

In this case, DVR transient and steady-state operation is surveyed. The optimum DVR location and distribution transformer tap setting as obtained in
Section 5.10 are bus 3 and 2.5%, respectively. The result is illustrated in Figure 5.29 in which DVR operation is started in a no load condition at 0.2 s. Then, at 1 s, buses start injecting in the second load level and at 2 s, start injecting in the first load level which is the high demand level. At 3 s, they start injecting in the third load level and at 4 s, start injecting in the fourth level which is the high generation level.

The DVR reference voltage is calculated in an online manner using (5.53), (5.58) and the already calculated ELI. The results show the effectiveness of DVR operation in all the load levels in maintaining the average voltage, $V_e$, close to the reference voltage of 1 pu, and settling time of about 400 ms is achieved in response to the step load variations. Over and under shoots are small and bus voltages are kept in the allowable range in most of the duration of transients. As observed in the plot, DVR cannot affect the upstream bus number 2, and it is only affected by network currents. Nevertheless, the network average voltage deviation in both the low demand and high generation levels is reduced compared to Figure 5.26(b) and is minimised because of the effect of both the optimum placement and online regulation. The minimised voltage deviations help in improving the efficiency of electric motor loads and reducing network losses. Moreover, this algorithm prevents the overvoltage protection from being triggered, and since the voltage deviations from 1 pu are controlled to be minimum, droop function is not enabled, and therefore, the reduction of power generation is avoided, and PVs can inject their maximum available power.
In Figure 5.30, DVR reference voltage, $V_{DVR}^{rms}$, and DVR output voltage as well as the output reactive power of DVR are plotted. The converter control algorithm has been able to follow the reference voltage in all the loads levels. The values of RMS reference voltage in different load levels and the maximum value of output reactive power are consistent with the results of optimisation for average voltage deviation minimisation which are already presented in Figure 5.18 and Table 5.6.
In the proposed approach renewable energy curtailment and overvoltage protection are avoided, because voltage rise is controlled. Figure 5.31 shows the DVR output voltage...
voltage, \( v_C(t) \), and reference voltage in transient from no load condition to load level 2 at 1 s. The designed converter controller in Chapter 4 is able to track the generated reference voltage.

![Figure 5.31 DVR output voltage and reference voltage](image)

**5.11.4 Case 4: Voltage Regulation with Minimum DVR Rating Performance**

The results of optimisation for DVR rating minimisation in Table 5.8 already showed that a DVR with limited power rating cannot minimise the average voltage deviation but is still effective in keeping bus voltages in the allowable range. In order to examine the effectiveness of the algorithm in this case, DVR output voltage is limited to resemble a lower rating DVR. Figure 5.20 shows the optimisation results for DVR rating minimisation in which optimum voltages for the entire load levels are obtained. It shows that in load level one, the maximum compensating voltage of 0.059466 pu is needed, and therefore, this voltage is considered as the voltage limit. The results in Figure 5.32 compared with Figure 5.29 show that the limited power rating increases the deviations as expected, but bus voltages remain in the allowable range.
Figure 5.32 (a) Voltage regulation with minimised DVR rating, and (b) average voltage deviation

Figure 5.33 shows the limited reference voltage for DVR output.

Figure 5.33 DVR reference RMS voltage with minimised DVR rating
Figure 5.34 shows the reactive power injection by DVR indicating the limited injection because of the minimised DVR rating.

![DVR Output Reactive Power](image)

Figure 5.34 DVR output reactive power with minimised DVR rating

### 5.11.5 Case 5: Harmonic Distortion Reduction Performance

In this case, harmonic current injection is added to all buses. Harmonic current magnitudes for odd numbered harmonics including 3rd, 5th, 7th and 9th harmonics are set as about 15, 12, 8 and 5 % of the nominal current injection of the bus for the fundamental content. Simulations are performed in load level 1 which introduces the highest voltage drops in the network. The voltage source of the network is assumed as stiff, and its internal impedance is not considered is the simulations. The Harmonic compensation algorithm compensates 3rd, 5th and 7th harmonics. 9th harmonic is not compensated, but as discussed in Sections 4.5.2 and 4.5.3, a zero reference voltage is commanded for this harmonic in order to eliminate the voltage drop at the output caused by the 9th harmonic content of the disturbance current.

Bus voltage THDs and average THD before and after compensation are plotted in Figure 5.35(a). THD is calculated by including all four selected harmonics. Buses start injecting at 0.3 s, and DVR compensation is turned on at 1 s. The compensation is performed by active power injection using (5.70) and the approximate ELI calculated by (5.63). The results show that DVR has provided some compensating harmonic content, and consequently, THD of downstream busses have been decreased. The average THD of network is decreased by 36.7%. In addition, the FFT of DVR output voltage in Figure 5.35(c) shows the effectiveness of the converter control algorithm in tracking the generated harmonic references.
Figure 5.35 (a) Bus voltage THDs and average THD with compensation using active power injection, (b) DVR compensating reference and output voltages, and (c) FFT of DVR output voltage
Figure 5.36 (a) Uncompensated voltage, (b) compensated voltage, and (c) FFT for bus 5 voltage

Figure 5.36(a) shows the voltage of bus number 5 which has the highest level of distortion, because it is the farthest bus from the voltage source. The compensated voltage of this bus is plotted in Figure 5.36(b) which indicates a less distorted...
voltage. The FFT in Figure 5.36(c) shows that the harmonic content for the compensated harmonics is decreased, and as expected, the uncompensated 9th harmonic has not introduced any voltage drops into the downstream network.

In addition, the reactive compensation using the real part of (5.68) is also performed. The results in Figure 5.37(a) show a reduction of about 33.3% in average THD that is less than the case with active power injection, as expected. The FFT of bus voltage number 5 shows an increased harmonic content compared to the previous case.

![Graph showing bus voltage THDs and average THD with compensation using only reactive power injection, and (b) FFT for bus voltage number 5](image)

5.12 CONCLUSIONS

In this chapter, the overvoltage issue of LV grids with high PV injection as well as the under-voltage issue caused by demand growth were considered, and a regulation algorithm by using DVR was proposed and applied in order to eliminate
the high bus voltage deviation issue. An optimisation algorithm was developed in which average yearly clustered load levels at buses in the network were used in order to find an optimum location for DVR and also an optimum setting for distribution transformer tap so that the desired voltage deviation with minimum DVR rating is achieved. The obtained optimum configuration values, including tap setting and DVR location, are fixed during the whole year. Therefore, the desired regulation is achieved with unchanged configuration during a year. The optimisation results were provided using a 6-bus LV network which proved the effectiveness of the proposed optimisation algorithm in finding an optimal solution for any practically defined objectives.

In addition, in order to have proper regulation for any bus loading and generation, a regulation method was proposed in which by using the calculated equivalent line impedance, online regulation of network is possible without the need for any communication links between buses and DVR. Since the ELI is calculated based on the average of its obtained values in all the clustered load levels, it can be used in any loading conditions at buses, and therefore, only one value is required to be calculated and used for regulation computations. Simulation results showed that the algorithm was able to regulate average bus voltages to the reference 1 pu in all loading conditions. Additionally, with reduced rating, DVR was still able to maintain bus voltages in the allowable range. Moreover, the algorithm was extended in order to reduce the average THD of the network by injecting compensating harmonic voltages by DVR. Simulation results showed the effectiveness of the algorithm in reducing the average THD of the network.

Furthermore, a comparison between shunt and series compensation was provided. The optimisation results for shunt compensation showed a higher required power rating for a similar regulation which showed a benefit of series compensation by DVR. In addition, the implications of extending the algorithms for three-phase applications were provided.
Chapter 6: Conclusions and Recommendations

The general conclusions and recommendations for future scopes of the work are presented in this chapter.

6.1 GENERAL CONCLUSIONS

The first aim of this thesis is to develop a new stable and online voltage quality improvement algorithm by using a series compensator for grids containing high photovoltaic (PV) penetration as well as high demand and harmonic injection. The second aim is to develop an improved optimisation algorithm for placement of the compensator in the network in order to minimise its power rating while minimising bus voltage deviations in the network. The third aim is designing a suitable converter as the compensator and developing improved reference tracking algorithm in order to control the output voltage of the series compensator which needs to follow harmonic references as well as a fundamental reference with minimum error and enough stability margins. The last aim is set for developing improved algorithms for synchronisation to the disturbed grid voltage which is required for proper and stable operation of most of grid-interfaced devices including the utilised compensator.

The first aim has been realised by placing a Dynamic Voltage Restorer (DVR) as a series compensator to inject a controlled amount of voltage to minimise the average voltage deviation of buses in the network so that high voltage rises by PV generation are avoided and high voltage drops caused by demand growth are compensated. The algorithm can also reduce voltage drops caused by harmonic power injection and reduce the Total Harmonic Distortion (THD) of bus voltages. This is a new method in which a pre-calculated equivalent line impedance value is used in order to estimate the average voltage deviation of buses using only local information of the compensator with no need for communication links between buses and DVR. An appropriate reference voltage for DVR is, then, calculated, and the quality improvement algorithm is performed in an online manner. The algorithm is able to regulate bus voltages and reduce the THD. Compared to other methods which result in loss of PV generation, the proposed structure makes the best use of PV generation.
The second aim has been accomplished by using a hybrid optimisation algorithm. A new approach for optimisation is proposed in which averaged clustered load levels of network buses and their durations are considered. Furthermore, in addition to finding an optimum place for DVR, finding a fixed optimum setting for distribution transformer tap is also included in the algorithm. The optimisation results help in finding the best configuration for the network to minimise the investment cost.

The third aim has been achieved by designing a feedback control algorithm using the Internal Model Principle (IMP) in order to control the output voltage of DVR to track a desired reference voltage. The designed control algorithm is also able to track harmonic references utilising stacked resonant compensators. A feedforward compensator is also used in order to improve the disturbance rejection of the control system. Pole placement technique is shown to be a good method for control parameter tuning. In addition, a model-based delay compensation method is used to free the control design from inclusion of the control loop delay introduced by digital controller computations. A new adaptive method is proposed in order to make the control system performance and delay compensation algorithm independent of plant parameter variations. The performance of control algorithm showed a desirable reference tracking and a stable performance.

The last aim has been fulfilled by the design of algorithms for synchronisation to the grid voltage. An algorithm using Moving Average Filter (MAF) and feedforward is developed in order to measure the angle of a disturbed voltage. The algorithm has been made adaptive to frequency variations by a new method for proper variation of MAF window length for effective rejection of undesired harmonic content. In addition, angle of harmonic voltages are also measured by designing a new stacked Phase-Locked Loop (PLL) structure. Furthermore, a new Frequency-Locked Loop (FLL) structure is also proposed which is able to reject harmonics unlike the previously presented FLL structures. The designed synchronisation algorithms showed desirable transient and steady-state performances in response to phase and frequency variations of the grid voltage.

However, the developed algorithms raise some new questions and recommendations for future research.
6.2 RECOMMENDATIONS FOR FUTURE WORK

Some scopes of future work for each chapter can be identified as follows.

6.2.1 Synchronisation Algorithms
- The integrated FLL and PLL structure designed in Section 3.6 is nonlinear system. It may be possible to derive a small-signal model for this structure so that controller tuning can be performed more effectively.

6.2.2 Converter Design and Reference Tracking Algorithms
- An algorithm for control of paralleled DVRs can be developed in order to increase the current rating of the compensator to be used in networks with high levels of demand and generation.
- Gain of resonance compensators sharply declines as the frequency varies. Therefore, they can be made adaptive to frequency variations so that controller tracking performance does not degrade with varying frequency of main voltage.
- The converter can be designed for three-phase applications, and its tracking control algorithm is modified to be able to follow a three-phase reference voltage including positive, negative and zero sequences.

6.2.3 Optimisation and Voltage Quality Improvement Algorithms
- DVR voltage angle can be included as a decision variable in optimisation. In this case, active power injection is also required by DVR. The results will be similar to the case for compensation with minimum DVR voltage in Section 5.5.2, because the optimisation will find the minimum rating which is obtained with minimum compensation voltage.
- In large networks, multiple DVRs can be used in different locations in order to have a better regulation and reduced power rating for each DVR. The optimisation algorithm and the load flow analysis must be manipulated to include multiple compensators. The equivalent line impedance concept needs more work to be used in a multiple DVR configuration.
- The optimisation can be performed with consideration of future demand and generation growth which needs a planning algorithm for forecasting.
the future growth of network. The optimisation can be applied to the predicted network to find an optimised rating and location for DVR so that it can operate more efficiently during the planned period.

- Three single-phase DVRs can be placed on three phases or a three-phase structure can be used in order to improve voltage and phase unbalances in three-phase networks. The compensation algorithm needs to be modified in order to generate appropriate positive, negative and zero sequence reference voltages.

- Protection is the main drawback of DVR usage in grids. The series connected compensator brings new protection challenges which must be considered and eliminated. More research is required on protection issues of this device to be able to use it commercially in low voltage (LV) grids.

- The issue on the reliability of the power system with the proposed regulation and voltage quality improvement algorithm using DVR could be surveyed, and statistical analyses can be performed to obtain the amount of influence on reliability.
Bibliography


[80] M. Mohammadi, "Voltage Dip Rating Reduction Based Optimal Location of DVR for Reliability Improvement of Electrical Distribution System,"


[140] S. M. Ami, "Power quality improvements in low voltage distribution networks containing distributed energy resources," PhD, School of Electrical Engineering and Computer Science, Queensland University of Technology (QUT), 2015.

Appendices

Appendix A

**Typhoon HIL and DSP interfacing**

Typhoon HIL400 emulator in Figure A.1 is an embedded HIL system for testing and rapid prototyping of PV inverters, active filters, motor drives and wind turbine converters. It offers a real-time HIL emulation system with 500 ns to 2 μs simulation time step as well as industrial controllers for power electronics. It can emulate power electronic components provided in its library including passive components, current and voltage sources, contactors, power switches, transformers and electric motors. It also provides 16 analogue output, 8 analogue inputs, 32 digital inputs, and 32 digital outputs for interfacing the emulated and control signals to the DSP control platform. Digital inputs of emulator can receive power switch gate signals and contactor commands from the controller, and analogue outputs can send the emulated signals to the controller.

The sources generate voltage and current signals which are used in the simulation and can also be sent to the analogue outputs. Their values can be configures as constant, AC with harmonics or arbitrary. In the arbitrary mode, a repetitive signal can be generated by listing the samples of one repetition of the desired signal in a text file.

Building the power electronics system model and performing test scenarios can be achieved as follows:

1. Defining converter model in the schematic editor and compiling circuit.
2. Running the model from the simulation control centre and changing sources, toggling contactors, loading machines as well as interfacing the emulated signals to TI DSP control platform via analogue and digital input and outputs.
3. Compiling, programming and running the TI DSP with desired control software.
Figure A.1 HIL emulation system, (a) pictured and (b) diagram [Courtesy of Typhoon HIL Inc.]

**HIL DSP Interface**

Typhoon HIL DSP Interface (TI Docking Station) in Figure A.2 is built for a family of TI DIMM 100 DSP cards (F280x and F2833x) to interface the TI controller to the Typhoon HIL emulator. All digital and analogue signals from/to HIL DSP Interface are routed directly between HIL analogue and digital I/O pins and TI controller. All HIL analog/digital I/O pins are also physically accessible via headers. In addition, the docking station contains on-board peripherals and external connectors for monitoring and debugging. It also features:
- JTAG connector with voltage level selection.
- 5 LEDs and 4 slide switches connected to HIL.
- 4 LEDs and 3 push buttons connected to TI DSP.
- BNC connectors for monitoring analogue outputs.
- Sixteen analogue outputs from HIL scaled from ±5V to DSP’s 0-3 V. Eight of them can be configured to scale HIL’s 0-5 V to DSP’s 0-3 V (unipolar). Practically, the analogue output range is ±4.5 V.

Figure A.2 TI Docking Station, (a) picture and (b) block diagram [Courtesy of Typhoon HIL Inc.]
Figure A.3 depicts an example for control system development by emulating a grid-interfaced inverter and interfacing the analogue and digital signals to the TI Docking Station.
Appendix B

List of Publications

The following papers are published or are under publication process from the results of this work.

**Journal Papers**


**Conference Papers**
